WHAT IS CLAIMED IS:

1. A method of semiconductor fabrication, comprising:

providing a substrate having a semiconductor fin;

forming a gate structure over the semiconductor fin;

forming a recess in the semiconductor fin adjacent the gate structure, wherein the recess is defined by a first sidewall, an opposing second sidewall and a bottom surface extending from the first sidewall to the opposing second sidewall, and wherein each of the first sidewall, the opposing second sidewall, and the bottom surface are interfaces with the semiconductor fin;

altering the first sidewall of the recess and the opposing second sidewall of the recess by forming a dielectric offset liner layer on the first and opposing second sidewalls of the recess~~a sidewall of the recess~~; ~~and~~

growing ~~an~~ a first epitaxial region in the recess, wherein the first epitaxial region interfaces a first surface and an opposing second surface of the dielectric offset liner layer and wherein the first epitaxial region is a strained epitaxial region, and wherein the first epitaxial region extends to a first height and the dielectric offset liner layer extends to a second height, the second height being greater than the first height such that an angle defined by an intersection between a top surface of the first epitaxial region and the first surface of the dielectric offset liner layer is less than 90 degrees;~~the altered sidewall of the recess and is a strained epitaxial region~~

after the growing of the first epitaxial region, removing the dielectric offset liner layer including the first surface and the opposing second surface of the dielectric offset liner layer; and

growing a second epitaxial region on and over the first epitaxial region after removing the dielectric offset liner layer.

2. The method of claim 1, wherein the altering the first and opposing second sidewalls ~~sidewall~~ of the recess includes forming ~~an~~ the dielectric offset liner layer by growing a dielectric material on the first and opposing second sidewalls of the recess.

~~3. The method of claim 2, wherein the epitaxial region interfaces the offset liner layer.~~

~~4. The method of claim 1, wherein the altering the sidewall of the recess includes performing an ion implantation process on the sidewall of the recess.~~

~~5. The method of claim 4, wherein the ion implantation process includes a tilt implant.~~

~~6. The method of claim 5, wherein the tilt implant is performed at an angle between approximately 10 degrees and approximately 60 degrees.~~

~~7. The method of claim 4, wherein the ion implantation includes implanting at least one of germanium, silicon, zenon, and carbon.~~

~~8. The method of claim 1, wherein the altering the sidewall of the recess includes providing a modified profile of the recess, wherein the modified profile includes an angle of less than approximately 90 degrees.~~

~~9~~3. A method of fabricating a semiconductor device, comprising:

forming a recess in a ~~semiconductor~~ substrate of semiconductor material, wherein the recess is defined by a first sidewall of the semiconductor material, a second sidewall of the semiconductor material, and a bottom surface of the semiconductor material;

forming an offset liner layer on the first and second sidewalls of the recess, wherein the offset liner layer has interfaces with the semiconductor material on the first and second sidewalls of the recess; wherein the offset liner layer has a dielectric composition~~sidewalls of the recess~~; and

growing ~~an~~ a first epitaxial region in the bottom surface in a bottom portion of the recess, wherein a top portion of the recess above the first epitaxial region is vacant after the growing the first epitaxial region;~~the epitaxial region has an interface with the offset liner layer~~

wherein the growing the first epitaxial region includes:

growing a first portion of the first epitaxial region such that the first portion has a direct interface to a lateral sidewall of the offset liner layer, wherein the lateral sidewall of the offset liner layer is substantially parallel to the first sidewall of the recess and wherein an angle defined by an intersection between a top surface of the first epitaxial region and the lateral sidewall of the offset liner layer is less than 90 degrees;

removing the offset liner layer thereby removing the direct interface between the first portion of the first epitaxial region and the offset liner layer, and

after removing the offset liner layer, growing a second portion of the first epitaxial region in the top portion of the recess filling the vacancy.

~~10~~4. The method of claim ~~9~~3, wherein the forming the offset liner layer includes forming a conformal layer on the substrate of semiconductor material and etching the conformal layer to provide the offset liner layer on the first and second sidewalls of the recess.

~~11~~5. The method of claim ~~9~~3, wherein the forming the offset liner layer includes growing the offset liner layer on the first and second sidewalls of the recess.

~~12. The method of claim 9, wherein the growing the epitaxial region includes growing a first portion of the epitaxial region, removing the offset liner layer, and after the removing the offset liner layer, growing a second portion of the epitaxial region.~~

~~13~~6. The method of claim ~~9~~3, wherein the first epitaxial region provides a source or drain region of the semiconductor device.

~~14~~7. The method of claim ~~9~~3, wherein the semiconductor device is a multi-gate fin-type device.

~~15~~8. The method of claim ~~9~~3, wherein the first epitaxial region is disposed in a fin structure, and wherein the first epitaxial region interposes a first gate structure and a second gate structure formed over the fin structure.

~~16. A semiconductor device, comprising:~~

~~a fin structure;~~

~~a first gate structure formed on the fin structure;~~

~~a strained epitaxial region formed in the fin structure, wherein the strained epitaxial region includes a first region of epitaxy having a top surface and an opposing bottom surface, wherein the bottom surface is concave in shape; and~~

~~a dielectric layer disposed between the epitaxial region and the fin.~~

~~17. The semiconductor device of claim 16, wherein the bottom surface of the first region of epitaxy directly interfaces with the fin structure.~~

~~18. The semiconductor device of claim 16, further comprising:~~

~~a second gate structure formed on the fin, wherein the strained epitaxial region interposes the first gate structure and the second gate structure, and wherein the first region of epitaxy includes a source/drain region associated with the first gate structure and a source/drain region associated with the second gate structure.~~

~~19. The semiconductor device of claim 16, wherein the first region of epitaxy is disposed on a second region of epitaxy, and wherein the bottom surface of the first region of epitaxy directly interfaces with the second region of epitaxy.~~

~~20. The semiconductor device of claim 19, wherein the first and second regions of epitaxy have different compositions.~~