ABSTRACT

A semiconductor device includes: first and second unit cell areas adjacent one another in a first direction; a third unit cell area adjacent the first unit cell area in a second direction; a tap cell area arranged with the first unit cell area along the first direction; a bit-line and complementary bit-line each extending in the second direction on a first surface of a substrate and connected to the first and third unit cell areas; and a word-line extending in the first direction on a second surface of the substrate and connected to the first and second unit cell areas. Each of the first to third unit cell areas includes: first and second inverters forming a latch circuit; and first and second pass transistors connecting the latch circuit to the bit-line and complementary bit-line. The tap cell area electrically connects the first and second pass transistors and the word-line.

FIG. 3