SEMICONDUCTOR MEMORY DEVICE

ABSTRACT

A memory cell with a small surface area is fabricated by forming source lines and data lines above and below and by running the channels to face up and down. The local data lines for each vertically stacked memory cell are connected to a global data line by way of separate selection by a molecular oxide semiconductor, and use of a large surface area is avoided by making joint use of peripheral circuits such as global data lines and sensing amplifiers by performing read and write operations in a timed multiplex manner. Moreover, data lines in multi-layers and memory cells (floating electrode cell) which are non-destructive with respect to readout are utilized to allow placement of memory cells at all intersecting points of word lines and data lines while having a folded data line structure. An improved noise tolerance is attained by establishing a standard threshold voltage for identical dummy cells even in any of the read verify, write verify and erase verify operations. A register to temporarily hold write data in a memory cell during writing is also used as a register to hold a flag showing that writing has ended during write verify. Also, a circuit comprised of one nMOS transistor is utilized as a means to change values on the write-end flag.

Fig. 51