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(54) A METHOD OF MAKING STATIC INDUCTION TRANSISTOR LOGIC

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 6-31-1, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to methods of making static induction transistor logic and to static induction transistor logic when made thereby.

According to one aspect of the present invention there is provided a method of making a semiconductor static induction transistor logic device having a source, a gate region with a relatively high impurity concentration of one type in a layer with a relatively low impurity concentration of opposite type, and a channel region, the method comprising forming the gate region with a reduced dimension portion adjacent a drain region and an increased dimension portion adjacent the source by an ion implantation technique.

In one embodiment the gate region is formed by a stepped ion implantation technique.

The ion implantation technique preferably comprises implanting ions from an ion beam and subsequently diffusing the ions into the said layer by a heating operation.

The method may include forming the source of N⁺ conductivity type material, the said layer of N⁺ conductivity type material, the gate region of P⁺ conductivity type material and the drain region of N⁺ conductivity type material.

Alternatively the method may include forming the source of P⁺ conductivity type material, the said layer of P⁺ conductivity type material, the gate region of N⁺ conductivity type material and the drain region of P⁺ conductivity type material.

According to a further aspect of the present invention there is provided static induction transistor logic when made by the method recited above.

The invention is illustrated, merely by

way of example, in the accompanying drawings, in which:—

Figure 1 is a schematic sectional view of conventional static induction transistor logic;

Figure 2 is a detailed view of a channel region of the conventional static induction transistor logic shown in Figure 1;

Figure 3 is a schematic diagram of diffusion potentials in the channel region of the conventional static induction transistor logic of Figure 1;

Figure 4 is a schematic sectional view of another type of conventional static induction transistor logic;

Figure 5 is a schematic sectional view of one embodiment of static induction transistor logic made by a method according to the present invention;

Figure 6 is a diagram illustrating ion distribution by an ion implantation technique;

Figure 7 (a) illustrates ion distribution resulting from a stepped ion implantation technique; and

Figure 7 (b) illustrates, in section, a gate region formed by a stepped ion implantation technique.

Throughout the drawings like parts have been designated by the same reference numerals.

Conventional static induction transistor logic, illustrated in Figure 1, comprises an injector 5 and a static induction transistor T for switching the conductive state between a substrate 1 acting as a source and a drain region 4, by controlling the height of a potential barrier as a result of changing the potential of a gate region 3 which is used as a barrier for carrier transfer, the barrier being at a given diffusion potential and being constituted by a junction between an epitaxial layer 2 having a relatively low impurity concentration formed on the substrate 1 by, for example, an epitaxial deposition technique, and the gate region 3 having an inverse relatively high impurity concentration and formed in the epitaxial layer 2.

The substrate 1 is, in this instance, of N⁺ conductivity type material, the epitaxial

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layer 2 is of N⁻ conductivity type material, the gate region 3 and the injector 5 are of P⁺ conductivity type material and the drain region 4 is of N⁺ type conductivity material. Hitherto, the gate region 3 has been formed by a heat-diffusion technique using boron and has had an arcuate shape with a radius r centred around ends A (Figure 2) of a mask (not shown) used during diffusion of the gate region. The radius r is also dependent upon the diffusion time. As a result, the distribution of diffusion potential at the junction between the gate region 3 and epitaxial layer 2 has had a distribution as shown by dotted lines in Figure 2. The diffusion potential increases in the direction of the arrows and is a maximum at a point P at a distance x from the substrate 1 as shown in Figure 3 which illustrates the diffusion potential in a plane B-B' of an intrinsic channel region between the gate regions. The point P is located at a distance from the substrate 1 so that when a positive bias (curve b) is applied to the gate region 3 and a positive bias (curve c) is applied to the gate region 4, it takes time for electrons injected from the substrate 1 into the epitaxial layer 2 to reach the point P by diffusion transfer. For this reason conventional static induction transistor logic is not suitable for high-frequency operation. In an attempt to move the point P closer to the substrate 1, the lower parts of a gate region 3' (Figure 4) having been formed during growing of the epitaxial layer, the remainder of the gate region being diffused into the epitaxial layer 2 after the completion of the growing thereof.

In the conventional static induction transistor logic, the point P is located at the narrowest portion inside the gate regions, so that in spite of improving the operating characteristics, the type of conventional static induction transistor logic illustrated in Figure 4 is complicated to make, manufacturing yield is reduced and the cost is increased.

Referring now to Figure 5 there is illustrated one embodiment of static induction transistor logic made by a method according to the present invention. The N⁺ conductivity type material of the substrate 1 has an impurity concentration of the order of 10^{18} , and the N⁻ conductivity type material of the epitaxial layer 2 has an impurity concentration of the order of 10^{15} . The epitaxial layer has a thickness of $4\text{ }\mu\text{m}$. The gate region 3 and the injector 5 are formed to have an enlarged portion closest to the substrate 1 by means of an ion implantation technique. The impurity concentration of the gate region 3 is of the order of 10^{18} and it has a depth of about $3.0\text{ }\mu\text{m}$ from the surface of the epitaxial layer 2. The channel region has a mini-

mum width W located at the depth of about $2\text{ }\mu\text{m}$ from the surface of the epitaxial layer 2. The drain region 4 has a thickness less than $1\text{ }\mu\text{m}$ and an impurity concentration of the order of 10^{19} . After the formation of the gate region and the drain region an oxide film and electrical wiring are formed to complete the static induction transistor logic but neither of these are shown in Figure 5.

The essential point of the present invention is the increased dimensions of the gate region adjacent the substrate 1 and the method of forming such a gate region will now be described.

Figure 6 is a diagram of the average projection range and standard deviation for boron ions injected into a silicon substrate with an energy of, for example, 1000 Kev. The boron ions penetrate to a mean depth of about $2\text{ }\mu\text{m}$ from the surface of the substrate with a Gaussian distribution having a standard deviation of about $0.1\text{ }\mu\text{m}$. Since the concentration of boron in the substrate can be controlled by the implanting time and ion beam current, the ion concentration at a given depth can be selectively determined. In this embodiment, initially, ions are implanted in the substrate at a depth of about $2\text{ }\mu\text{m}$ with a high impurity concentration (about 10^{19}) and subsequently are implanted at depths of $1.2\text{ }\mu\text{m}$, $0.6\text{ }\mu\text{m}$ and $0.2\text{ }\mu\text{m}$ successively at comparatively low impurity concentrations (10^{17}) as shown in Figure 7(a). These implanting operations are performed through the same mask, and therefore the shapes of the implanted areas approximate to those as shown by the reference numerals 31, 32, 34 respectively in Figure 7(b). That is to say, the implanted areas are concentric although there is some expansion in the case where the impurity concentration is increased. After the impurities have been implanted in the substrate, electric activation and diffusion from the implanted areas is effected by an annealing operation. Diffusion progresses from the highest concentration area, namely area 31, to an area 31' and from the areas 32, 33, 34 to areas 32', 33', 34' respectively so that the gate region has the cross-sectional shape shown in Figure 5.

As described above, the gate region is formed by a stepped ion implantation technique so that the channel region has a minimum width close to the substrate 1 and so that the point of maximum diffusion potential at the junction between the gate region 3 and the epitaxial layer 2 is close to the substrate. In the embodiment shown in Figure 5, the point of maximum diffusion potential is $2\text{ }\mu\text{m}$ from the substrate. Accordingly, when a positive voltage is applied to the gate region 3 and a positive bias is applied to the drain region 4 elec-

trons injected from the substrate 1 reach the potential barrier faster than the conventional static induction transistor logic shown in Figure 1 and after crossing the potential barrier drift to the drain region.

From the above it will be appreciated that the static induction transistor logic shown in Figure 5 has an improved speed of operation, i.e. it will operate at higher frequencies than conventional static induction transistor logic, and has decreased parasitic capacity since it uses relatively low impurity concentration regions. The fact that the distance from the substrate 1 to the potential barrier is relatively small decreases the probability of electrons from the substrate recombining with holes from the gate region in the channel region and so the equivalent resistance is relatively very small and the chances of an electron from the substrate reaching the drain region becomes relatively high. On the other hand, the minimum width W of the channel region can be easily controlled to close tolerances since it is not dependent upon or influenced by the thickness of the drain region 4 as in the conventional static induction transistor logic of Figure 1. Consequently, the height of the potential barrier can be increased and the equivalent resistance when there is no bias on the gate region 3, can be increased. Thus the voltage amplitude of the output is very close to the bias voltage between the substrate 1 and the drain region 4 so that the static induction transistor logic of Figure 5 is ideally suited to performing logic functions.

The present invention has been described in relation to Figure 5 where the epitaxial layer 2 is of N⁻ conductivity type material and the substrate 1 is of N⁺ conductivity type material. However the substrate may be of P⁺ conductivity type material, the epitaxial layer of P⁻ conductivity type material and the gate region of N⁺ conductivity type material. Furthermore, whilst a stepped ion implantation technique has been described it will be appreciated that a similar effect can be achieved by a single ion implantation technique if the distance between the substrate 1 and the drain region is reduced and the drain region is made sufficiently thin.

WHAT WE CLAIM IS:—

1. A method of making a semiconductor static induction transistor logic device having a source, a gate region with a relatively high impurity concentration of one type in a layer with a relatively low impurity concentration of opposite type, and a channel region, the method comprising forming the gate region with a reduced dimension portion adjacent a drain region and an increased dimension portion adjacent the source by an ion implantation technique.

2. A method as claimed in Claim 1 in which the gate region is formed by a stepped ion implantation technique.

3. A method as claimed in Claim 1 or 2 in which the ion implantation technique comprises implanting ions from an ion beam and subsequently diffusing the ions into the said layer by a heating operation.

4. A method as claimed in any preceding claim including forming the source of N⁺ conductivity type material, the said layer of N⁻ conductivity type material, the gate region of P⁺ conductivity type material and the drain region of N⁺ conductivity type material.

5. A method as claimed in any of Claims 1 to 3 including forming the source of P⁺ conductivity type material, the said layer of P⁻ conductivity type material, the gate region of N⁺ conductivity type material and the drain region of P⁺ conductivity type material.

6. A method of making a semiconductor static induction transistor logic device substantially as herein described with reference to Figures 5 and 7 of the accompanying drawings.

7. A semiconductor static induction transistor logic device when made by a method as claimed in any preceding claim.

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1. A method of making a semiconductor static induction transistor logic device having a source, a gate region with a relatively high impurity concentration of one type in a layer with a relatively low impurity concentration of opposite type, and a channel region, the method comprising forming the gate region with a reduced dimension portion adjacent a drain region and an increased dimension portion adjacent the source by an ion implantation technique.

2. A method as claimed in Claim 1 in which the gate region is formed by a stepped ion implantation technique.

3. A method as claimed in Claim 1 or 2 in which the ion implantation technique comprises implanting ions from an ion beam and subsequently diffusing the ions into the said layer by a heating operation.

4. A method as claimed in any preceding claim including forming the source of N⁺ conductivity type material, the said layer of N⁻ conductivity type material, the gate region of P⁺ conductivity type material and the drain region of N⁺ conductivity type material.

5. A method as claimed in any of Claims 1 to 3 including forming the source of P⁺ conductivity type material, the said layer of P⁻ conductivity type material, the gate region of N⁺ conductivity type material and the drain region of P⁺ conductivity type material.

6. A method of making a semiconductor static induction transistor logic device substantially as herein described with reference to Figures 5 and 7 of the accompanying drawings.

7. A semiconductor static induction transistor logic device when made by a method as claimed in any preceding claim.

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