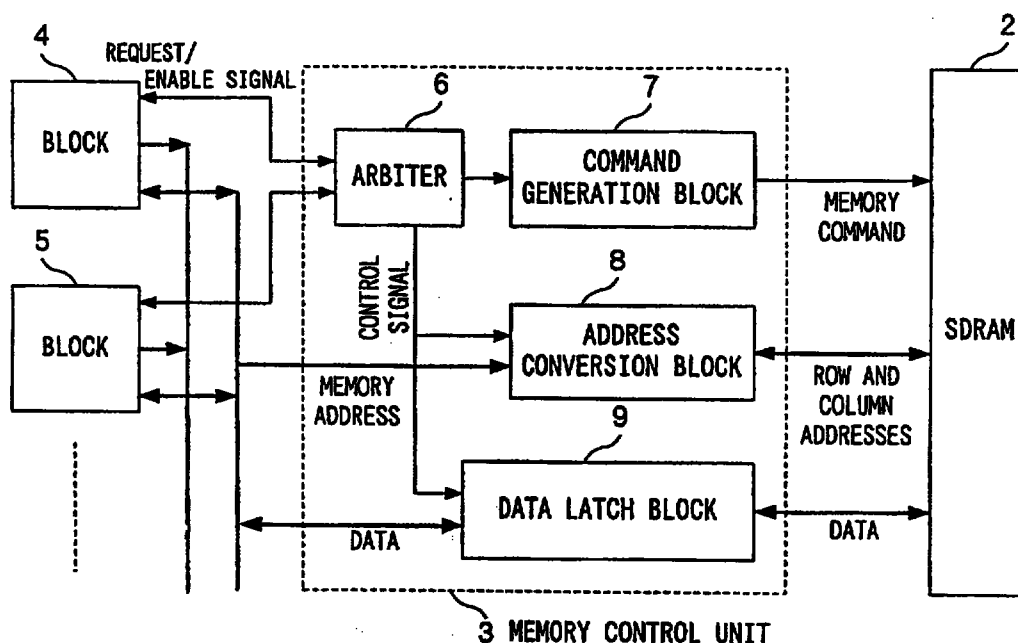




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(54) Title: MEMORY CONTROL UNIT



(57) Abstract

To provide a memory control unit which prevents continuous accesses to the same bank of SDRAM to increase its processing speed. The memory control unit (3) of the present invention controls SDRAM (2) which has two banks 0, 1 and can be continuously accessed in multiple-bank mode in which address inputs to the banks 0, 1 are seamlessly alternated between the banks by precharging the banks individually. The memory addresses provided by a block (4, 5) accessing the SDRAM (2) through the memory control unit (3) are converted into addresses such that the memory addresses are input to the banks of the SDRAM (2) alternately.