REDUCING CPU AND BUS POWER WHEN RUNNING IN POWER-SAVE MODES

BACKGROUND OF THE INVENTION

[0001] An apparatus containing a processor may have different modes of operation, the different modes representing a different trade-off between power consumption and performance.

[0002] In one exemplary mode of operation ("performance" mode), internal resources of the apparatus, including the processor, may be operated for high performance that may result in high power consumption.

[0003] In another exemplary mode of operation ("power-save" mode), internal resources of the apparatus, including the processor, may be operated for low power consumption while maintaining a predetermined performance for this mode of operation.

[0004] A processor may comprise a core constrained to have a lowest of core clock signal frequencies no lower than a predetermined multiple of a lowest of bus clock signal frequencies of a bus coupled to the processor. As higher bus clock signal frequencies become possible, this raises the lower limit to which the core clock signal frequencies can be reduced in power-save mode, thus hampering the efforts to reduce power consumption in power-save mode.

[0005] It would be beneficial to reduce power consumption while the apparatus operates in power-save mode, while maintaining or improving the performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

[0007] FIG. 1 is a simplified block diagram of an apparatus comprising a processing system in accordance with some embodiments of the present invention;

[0008] FIG. 2 is a simplified block-diagram illustration of a processing system, in accordance with some embodiments of the present invention; and

[0009] FIG. 3 is a simplified block-diagram illustration of an apparatus comprising a processing system, in accordance with other embodiments of the present invention; and

[0010] FIG. 4 is a simplified block-diagram illustration of a processor, in accordance with some embodiments of the present invention.

[0011] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[0012] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

[0013] It should be understood that embodiments of the present invention may be used in any apparatus having a processor. Although the present invention is not limited in this respect, the apparatus may be a portable device that may be powered by a battery. Non-limiting examples of such portable devices include laptop and notebook computers, mobile telephones, personal digital assistants (PDA), and the like. Alternatively, the apparatus may be a non-portable device, such as, for example, a desktop computer.

[0014] As shown in FIG. 1, according to some embodiments of the present invention, an apparatus 2 may comprise a processing system 4 and a power supply unit 6. Apparatus 2 may optionally comprise an antenna 8. Well-known components and circuits of apparatus 2 and processing system 4 are not shown in FIG. 1 so as not to obscure the invention.

[0015] Processing system 4 may comprise a processor 10 and an interface controller 20. Although the present invention is not limited in this respect, processor 10 may be, for example, a central processing unit (CPU), a digital signal processor (DSP), a reduced instruction set computer (RISC), a complex instruction set computer (CISC) and the like. Moreover, processor 10 may be part of an application specific integrated circuit (ASIC). Although the present invention is not limited in this respect, interface controller 20 may be, for example, a bus bridge, a peripheral component interconnect (PCI) north bridge, a PCI south bridge, an accelerated graphics port (AGP) bridge, a memory interface device and the like, or a combination thereof. Moreover, interface controller 20 may be part of an application specific integrated circuit (ASIC) or part of a chip set.

[0016] Processor 10 may comprise a core 12 and a core phase locked loop (PLL) 14. Core PLL 14 may generate one or more core clock signals 16 used by core 12 from a system clock signal 18.

[0017] Processor 10 and interface controller 20 may comprise a bus interface 13 and a bus interface 23, respectively, and may use them to generate and sample data, address and control signals of a bus 30.

[0018] Processor 10 and interface controller 20 may comprise a bus PLL 15 and a bus PLL 25, respectively. Bus PLL 15 and bus PLL 25 may use system clock signal 18 to generate clock signals 17 and clock signals 27, respectively. Bus interface 13 and bus interface 23 may use clock signals 17 and 27, respectively, to generate and sample data, address and control signals of bus 30.

[0019] Since they are derived from system clock signal 18, clock signals 16, 17 and 27 may maintain fixed phase relations with system clock signal 18, and consequently with one another. Moreover, the phase relations between clock signals 16, 17, and 27 may be used to generate and sample data, address and control signals of bus 30.

[0020] It will be appreciated by persons of ordinary skill in the art that the performance of processing system 4 may be related to the performance of processor 10, which may be related to the performance of core 12, which may be related to the frequencies of core clock signals 16. The performance of processing system 4 may also be related to the frequencies at which data, address and control signals of bus 30 are generated and sampled. Consequently, in a performance mode of operation, it may be desired to have clock signals 16, 17 and 27 oscillating at high frequencies.

[0021] In contrast, in a power-save mode of operation, it may be desired to have core clock signals 16 oscillating at low frequencies so the power consumption of core 12 of processor 10 is lower than in the performance mode of operation, while still supporting a predetermined performance of processing system 4 for this mode of operation.

[0022] However, due to design constraints, the frequencies of core clock signals 16 may be constrained to be at least a predetermined multiple of the lowest frequency of clock signals 17. For example, core clock signals 16 may be constrained to oscillate at at least six times the lowest frequency of clock signals 17, although the present invention is not

limited in this respect. If clock signals 17 were to oscillate at the same frequencies both in performance mode and in power-save mode, then in power-save mode, core clock signals 16 would be constrained to oscillate at frequencies that may lead core 12 to produce higher performance (and higher power-consumption) than necessary to support the predetermined performance of processing system 4 for power-save mode.

[0023] Therefore, in order to enable core clock signals 16 to oscillate at low frequencies, clock signals 17 (and hence clock signals 27) may be generated at even lower frequencies, if that is possible while still supporting the predetermined performance of processing system 4 for power-save mode. If the frequencies of clock signals 17 and 27 are reduced relative to the frequencies that they have in performance mode, this may reduce the power consumption associated with bus interface 13, bus interface 23 and bus 30 relative to that in the performance mode of operation.

[0024] For example, in one embodiment of the present invention, system clock signal 18 may oscillate at a lower frequency in power-save mode than in performance mode. Since clock signals 16, 17 and 27 are derived from system clock signal 18, they may scale with system clock signal 18. For example, system clock signal 18 may oscillate at 200MHz in performance mode and at 100MHz in power-save mode. The lowest frequency of clock signal 17 may be 200MHz in performance mode and 100MHz in power-save mode, enabling core clock signals 16 to oscillate at as low as 600MHz in power-save mode, using an example where the core clock signals are constrained to oscillate at frequencies no lower than six times the lowest frequency of the bus clock signals. However, in this embodiment, as processing system 4 changes from one mode to another, there may be a period of time until core PLL 18 and bus PLLs 15 and 25 relock onto the new frequency of system clock signal 18, and therefore bus 30 will be idle during this time. For example, during the relock time, processor 10 may not be able to respond to interrupts and snoops. This may limit the occasions where a switch between performance mode and power-save mode may be performed. Although the present invention is not limited in this respect, in some cases the relock time of PLLs 18, 15 and 25 may be approximately 5 to 30 microseconds.

[0025] In other embodiments of the present invention, described hereinbelow with respect to FIG. 2, the frequency of system clock signal 18 does not vary between performance mode and power-save mode.

[0026] Power supply unit 6 may provide power to core 12 via a power trace 61. Moreover, power supply unit 6 may provide power to bus interface 13 and to bus interface 23 via a power trace 62.

[0027] It will be appreciated by persons of ordinary skill in the art that the power consumption associated with core 12 of processor 10 increases as the voltage on power trace 61 increases, and the power consumption associated with bus interface 13, bus 30 and bus interface 23 increases as the voltage on power trace 62 increases. Consequently, it may be desired to lower the voltage on power traces 61 and 62 when apparatus 2 is in the power-save mode of operation. In order to enable lowering the voltage on power trace 62, bus interface 13 and bus interface 23 may be designed to use a low voltage level for a low frequency mode, such as, for example, the power-save mode, and a higher voltage level for a high frequency mode, such as, for example, the performance mode. It will be appreciated by persons of ordinary skill in the art that the lower the frequencies of core clock signals 16, the lower power supply unit 6 may reduce the voltage on power trace 61. Similarly, the lower the frequencies of clock signals 17 and 27, the lower power supply unit 6 may reduce the voltage on power trace 62.

[0028] It will also be appreciated by persons of ordinary skill in the art that frequency changes in clock signals involve some stabilization time. Therefore, when processor 10 changes the frequency of clock signals 17 and core clock signals 16 and instructs interface controller 20 to change the frequency of clock signals 27, there may be a period of time where the frequencies and phases of clock signals 16, 17 and 27 are not synchronized and therefore are inadequate for the operation of bus 30. Although the present invention is not limited in this respect, this period of time may be a few system clock signals, equivalent in some exemplary processors to approximately 10 – 40 nanoseconds. Consequently, it will be desirable to have a handshake between processor 10 and interface controller 20 when changing the frequency of clock signals 16, 17 and 27.

[0029] For example, processor 10 may send a signal to interface controller 20 to indicate a change from performance mode to power-save mode. This signal may be a new sideband signal from processor 10 to interface controller 20. Alternatively, an existing signal from interface controller 20 to processor 10 may be made bi-directional to support the functionality of processor 10 indicating a mode change to interface controller 20. Moreover, both processor 10 and interface controller 20 may refrain from using bus 30 for a predefined period of time following this indication to allow both processor 10 and interface controller 20 to complete internal changes and to be ready to accept and send transactions in the new mode.

[0030] FIG. 2 is a simplified block-diagram illustration of processing system 4, in accordance with some embodiments of the present invention.

[0031] Clock signals 17 of processor 10 may comprise clock signal 17A, clock signal 17B and clock signal 17C, which may be used, for example, by bus interface 13 to generate and sample control, address and data signals, respectively, over bus 30.

[0032] Similarly, clock signals 27 of interface controller 20 may comprise clock signal 27A, clock signal 27B and clock signal 27C, which may be used, for example, by bus interface 23 to generate and sample control, address and data signals, respectively, over bus 30.

[0033] Clock signals 17A, 17B and 17C may have fixed frequency relations with one another. For example, clock signal 17C may oscillate at twice the frequency of clock signal 17B, and clock signal 17B may oscillate at twice the frequency of clock signal 17A. Moreover, clock signals 17A, 17B and 17C may maintain fixed phase relations with one another.

[0034] Similarly, clock signals 27A, 27B and 27C may have fixed frequency relations with one another. For example, clock signal 27C may oscillate at twice the frequency of clock signal 27B, and clock signal 27B may oscillate at twice the frequency of clock signal 27A. Moreover, clock signals 27A, 27B and 27C may maintain fixed phase relations with one another.

[0035] Bus PLL 15 of processor 10 may comprise a bus PLL core 150 and frequency dividers 151, 152 and 153. Bus PLL core 150 may receive system clock signal 18 as an

input and may generate a clock signal 154, which may maintain fixed phase relations with system clock signal 18 and with core clock signals 16. Clock signal 154 may oscillate at the same frequency in performance mode and in power-save mode, so that bus PLL core 150 may remain locked to system clock signal 18. Frequency dividers 151, 152 and 153 may receive clock signal 154 and may divide it to generate clock signal 17A, clock signal 17B and clock signal 17C, respectively. Therefore, clock signal 154, which is generated from system clock signal 18 and divided in order to generate clock signals 17A, 17B and 17C, may be considered an intermediate clock signal. Clock signal 154 may be internal to bus PLL 15, although the present invention is not limited in this respect. Clock signals 17A, 17B and 17C may maintain fixed phase relations with clock signal 154, with system clock signal 18 and with core clock signals 16.

[0036] As an example, in performance mode, clock signal 154 may oscillate at 1600MHz, and frequency dividers 151, 152 and 153 may divide clock signal 154 by eight, four and two, respectively, so that clock signals 17A, 17B and 17C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively. Core clock signals 16 may oscillate at 3000MHz, which is more than six times the frequency of clock signal 17A.

[0037] It may be possible for core 12 to support the predetermined performance of processing system 4 in power-save mode when core clock signals 16 oscillate at 600 MHz, and for bus interface 13, bus 30 and bus interface 23 to support the predetermined performance of processing system 4 in power-save mode when clock signal 17A oscillates at 100MHz.

[0038] Therefore, in power-save mode, clock signal 154 may still oscillate at 1600MHz, and frequency dividers 151, 152 and 153 may divide clock signal 154 by sixteen, eight and four, respectively, so that clock signals 17A, 17B and 17C oscillate at frequencies of 100MHz, 200MHz and 400MHz, respectively. Core clock signals 16 may then oscillate at frequencies as low as 600MHz, while still satisfying the constraint that the frequencies of core clock signals 16 are at least six times the frequency of clock signal 17A.

[0039] A frequency control signal 156 of processor 10 may be coupled to frequency dividers 151, 152 and 153, and may be used to change their frequency division between eight, four and two, respectively, in performance mode, and sixteen, eight and four,

respectively, in power-save mode. Although the present invention is not limited in this respect, the idle time in which the digital frequency dividers are changed may be approximately 2 – 8 clock cycles of system clock signal 18, equivalent in some exemplary processors to approximately 1 – 20 nanoseconds.

[0040] Although the present invention is not limited in this respect, in the exemplary processing system of FIG. 2, the frequencies of clock signal 27A, clock signal 27B and clock signal 27C may match the frequencies of clock signal 17A, clock signal 17B and clock signal 17C, respectively, both in the performance mode and in the power-save mode.

[0041] Bus PLL 25 of interface controller 20 may comprise a bus PLL core 250 and frequency dividers 251, 252 and 253. Bus PLL core 250 may receive system clock signal 18 as an input and may generate a clock signal 254, which may maintain fixed phase relations with system clock signal 18. Clock signal 254 may oscillate at the same frequency in performance mode and in power-save mode, so that bus PLL core 250 may remain locked to system clock signal 18. Frequency dividers 251, 252 and 253 may receive clock signal 254 and may divide it to generate clock signal 27A, clock signal 27B and clock signal 27C, respectively. Therefore, clock signal 254, which is generated from system clock signal 18 and divided in order to generate clock signals 27A, 27B and 27C, may be considered an intermediate clock signal. Clock signal 254 may be internal to bus PLL 25, although the present invention is not limited in this respect. Clock signals 27A, 27B and 27C may maintain fixed phase relations with clock signal 254, with system clock signal 18 and with clock signals 17A, 17B and 17C of processor 10.

[0042] In performance mode, clock signal 254 may oscillate at 1600MHz, and frequency dividers 251, 252 and 253 may divide clock signal 254 by eight, four and two, respectively, so that clock signal 27A, clock signal 27B and clock signal 27C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively.

[0043] In power-save mode, clock signal 254 may still oscillate at 1600MHz, and frequency dividers 251, 252 and 253 may divide clock signal 254 by sixteen, eight and four, respectively, so that clock signal 27A, clock signal 27B and clock signal 27C oscillate at frequencies of 100MHz, 200MHz and 400MHz, respectively.

[0044] A frequency control signal 256 of interface controller 20 may be connected to frequency dividers 251, 252 and 253, and may be used to change their frequency division between eight, four and two, respectively in performance mode, and sixteen, eight and four respectively in power-save mode.

[0045] In an alternate embodiment of the present invention, in both performance mode and power-save mode, frequency dividers 151, 152 and 153 may divide clock signal 154 by eight, four and two, respectively, so that when clock signal 154 oscillates at 1600MHz, clock signal 17A, clock signal 17B and clock signal 17C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively. There is no need for frequency control signal 156 in this alternate embodiment. Rather, in power-save mode, bus interface 13 may further divide clock signal 17A, clock signal 17B and clock signal 17C to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz, respectively. Alternatively, bus interface 13 may use masking logic to decide which edges of clock signals 17A, 17B and 17C to use, based on the mode, to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz in power-save mode.

[0046] In this alternate embodiment, in both performance mode and power-save mode, frequency dividers 251, 252 and 253 may divide clock signal 254 by eight, four and two, respectively, so that when clock signal 254 oscillates at 1600MHz, clock signal 27A, clock signal 27B and clock signal 27C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively. There is no need for frequency control signal 256 in this alternate embodiment. Rather, in power-save mode, bus interface 23 may further divide clock signal 27A, clock signal 27B and clock signal 27C to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz, respectively. Alternatively, bus interface 23 may use masking logic to decide which edges of clock signals 27A, 27B and 27C to use, based on the mode, to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz in power-save mode.

[0047] When the oscillation frequency of system clock signal 18 is less than or equal to the oscillation frequency of clock signal 17A and clock signal 27A, then there is no

difficulty to synchronize clock signal 17A and clock signal 27A to have a desired fixed phase relationship with each other.

[0048] However, when the oscillation frequency of system clock signal 18 is higher than the oscillation frequency of clock signal 17A and clock signal 27A, there may be more than one way for clock signal 17A and clock signal 27A to maintain fixed phase relations with system clock signal 18. For example, system clock signal 18 may oscillate at 200MHz, and in power-save mode, clock signal 17A and clock signal 27A may oscillate at 100 MHz. Even if clock signal 17A and clock signal 27A each maintain the same fixed phase relationship with system clock signal 18, there are four different fixed phase relationships possible between clock signal 17A and clock signal 27A, namely 0, $\pi/2$, π, and $3\pi/2$ radians. In order to set the fixed phase relation between clock signal 17A and clock signal 27A to be that desired by processing system 4, processor 10 may send a signal (not shown) to interface controller 20 when changing the frequency of clock signal 17A. This signal may be part of the handshake referred to hereinabove.

[0049] As shown in FIG. 3, according to some embodiments of the present invention, apparatus 2 may comprise a processing system 4 comprising a processor 10 having a PLL 35 for generating core clock signals 16 and clock signals 17 from system clock signal 18. As shown in FIG. 4, PLL 35 may comprise PLL core 150 and frequency dividers 151, 152 and 153. As with the embodiment described hereinabove with respect to FIG. 2, PLL core 150 may receive system clock signal 18 as an input and may generate clock signal 154, and frequency dividers 151, 152 and 153 may receive clock signal 154 and may divide it to generate clock signal 17A, clock signal 17B and clock signal 17C, respectively. Unlike the embodiment described hereinabove with respect to FIG. 2, PLL 35 may also comprise a frequency divider 355 to receive clock signal 154 and to divide it to generate a single core clock signal 16. If there are more than one core clock signals 16, then PLL 35 may comprise a corresponding number of frequency dividers to receive clock signal 154 and to divide it to generate core clock signals 16.

[0050] As an example, in performance mode, clock signal 154 may oscillate at 4800MHz, and frequency divider 355 may divide it by 1, so that core clock signal 16 oscillates at 4800MHz. Frequency dividers 151, 152 and 153 may divide clock signal

154 by twenty-four, twelve and six, respectively, so that clock signals 17A, 17B and 17C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively.

[0051] As an example, in power-save mode, clock signal 154 may still oscillate at 4800MHz, so that PLL core 150 may remain locked to system clock signal 18, and frequency divider 355 may divide it by 8, so that core clock signal 16 oscillates at 600MHz. Frequency dividers 151, 152 and 153 may divide clock signal 154 by forty-eight, twenty-four and twelve, respectively, so that clock signals 17A, 17B and 17C oscillate at frequencies of 100MHz, 200MHz and 400MHz, respectively.

[0052] Frequency control signal 156 of processor 10 may be coupled to frequency dividers 151, 152 and 153, and may be used to change their frequency division between twenty-four, twelve and six, respectively, in performance mode, and forty-eight, twenty-four and twelve, respectively, in power-save mode. Similarly, a frequency control signal 356 of processor 10 may be coupled to frequency divider 355 to change its frequency division between 1 in performance mode and 6 in power-save mode.

[0053] In an alternate embodiment of the present invention, in both performance mode and power-save mode, frequency dividers 151, 152 and 153 may divide clock signal 154 by twenty-four, twelve and six, respectively, so that when clock signal 154 oscillates at 4800MHz, clock signal 17A, clock signal 17B and clock signal 17C oscillate at frequencies of 200MHz, 400MHz and 800MHz, respectively. There is no need for frequency control signal 156 in this alternate embodiment. Rather, in power-save mode, bus interface 13 may further divide clock signal 17A, clock signal 17B and clock signal 17C to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz, respectively. Alternatively, bus interface 13 may use masking logic to decide which edges of clock signals 17A, 17B and 17C to use, based on the mode, to produce clock signals oscillating at frequencies of 100MHz, 200MHz and 400MHz in power-save mode.

[0054] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are

intended to cover all such modifications and changes as fall within the true spirit of the invention.

[0055] What is claimed is:

1. A method comprising:

generating an intermediate clock signal while locked to a system clock signal of an apparatus having a processor;

in a first mode, dividing said intermediate clock signal to generate one or more bus clock signals at a first set of one or more bus frequencies for a bus coupled to said processor; and

in a second mode, dividing said intermediate clock signal to generate said one or more bus clock signals at a second set of one or more bus frequencies, wherein a lowest of said second set is higher than a lowest of said first set.

2. The method of claim 1, further comprising:

in said first mode, generating one or more core clock signals at a first set of core frequencies for a core of said processor, wherein said first set of core frequencies are no lower than a predetermined multiple of said lowest of said first set of bus frequencies; and

in said second mode, generating said one or more core clock signals at a second set of core frequencies, wherein a lowest of said second set of core frequencies is lower than said predetermined multiple of said lowest of said first set of bus frequencies but no lower than said predetermined multiple of said lowest of said second set of bus frequencies.

3. The method of claim 2, wherein generating said one or more core clock signals at said first set of core frequencies comprises generating said first set of core frequencies sufficiently high to enable said processor to support a higher performance of said apparatus than that supported by said second set of core frequencies.

4. The method of claim 2, wherein generating said one or more core clock signals at said first set of core frequencies includes dividing said intermediate clock signal and generating said one or more core clock signals at said second set of core frequencies includes dividing said intermediate clock signal.

5. The method of claim 1, wherein dividing said intermediate clock signal to generate said one or more bus clock signals at said second set of bus frequencies comprises:

dividing said intermediate clock signal to generate said one or more bus clock signals at said first set of bus frequencies; and

using masking logic to select which edges of said one or more bus clock signals at said first set of bus frequencies to use to produce said one or more bus clock signals at said second set of bus frequencies.

6. The method of claim 1, further comprising:

in said second mode, supplying a lower voltage to an interface to said bus than that which supports said interface in said first mode.

7. A method comprising:

in a power-save mode of an apparatus having a processor and a bus, generating one or more bus clock signals having a lowest frequency that is lower than a lowest frequency of one or more bus clock signals in a performance mode of said apparatus, so as to enable a core of said processor to have a core clock signal frequency that is lower than a predetermined multiple of said lowest frequency of one or more bus clock signals in said performance mode even though said core is constrained to have core clock signal frequencies no lower than said predetermined multiple of a lowest of bus clock signal frequencies.

8. The method of claim 7, wherein generating said one or more bus clock signals comprises:

generating an intermediate clock signal from a system clock signal; and

dividing said intermediate clock signal to produce said one or more bus clock signals.

9. The method of claim 7, wherein generating said one or more bus clock signals comprises:

generating a first intermediate clock signal from a system clock signal;

dividing said first intermediate clock signal to produce one or more second intermediate clock signals; and

using masking logic to select which edges of said one or more second intermediate clock signals to use to produce said one or more bus clock signals.

10. The method of claim 7, further comprising:

supplying a lower voltage to an interface to said bus than that which supports said interface in performance mode.

11. An apparatus comprising:

a processor to be coupled to a bus, whose core is constrained to have one or more core clock signal frequencies no lower than a predetermined multiple of a lowest of one or more bus clock signal frequencies for one or more clock signals of said bus,

wherein said processor is, in a power-save mode of said apparatus, to generate one or more bus clock signals whose lowest frequency is lower than a lowest frequency of said one or more bus clock signals in a performance mode of said apparatus.

12. The apparatus of claim 11, wherein said processor further comprises:

a phase locked loop to generate an intermediate clock signal from a system clock signal, said phase locked loop including one or more digital frequency dividers to divide said intermediate clock signal in order to generate said one or more bus clock signals.

13. The apparatus of claim 12, wherein said phase locked loop further comprises one or more additional digital frequency dividers to divide said intermediate clock signal in order to generate one or more core clock signals for said core.

14. The apparatus of claim 12, wherein said processor further comprises:

another phase locked loop to generate one or more core clock signals for said core from said system clock signal.

15. An apparatus comprising:

a processing system including at least:

a bus; and

a processor coupled to said bus, whose core is constrained to have one or more core clock signal frequencies no lower than a predetermined multiple of a lowest of one or more bus clock signal frequencies for one or more clock signals of said bus,

wherein said processor is, in a power-save mode of said apparatus, to generate one or more bus clock signals whose lowest frequency is lower than a lowest frequency of said one or more bus clock signals in a performance mode of said apparatus.

16. The apparatus of claim 15, wherein said processor further comprises:

a phase locked loop to generate an intermediate clock signal from a system clock signal of said processing system, said phase locked loop including one or more digital frequency dividers to divide said intermediate clock signal in order to generate said one or more bus clock signals.

17. The apparatus of claim 16, wherein said phase locked loop further comprises one or more additional digital frequency dividers to divide said intermediate clock signal in order to generate one or more core clock signals for said core.

18. The apparatus of claim 16, wherein said processor further comprises:

another phase locked loop to generate one or more core clock signals for said core from said system clock signal.

19. The apparatus of claim 15, wherein said processing system further comprises:

a bus interface to receive said one or more bus clock signals.

20. The apparatus of claim 19, further comprising:

a power supply unit to supply a lower voltage to said bus interface than that which supports said performance mode.

21. An apparatus comprising:

an antenna; and

a processing system including at least:

a bus; and

a processor coupled to said bus, whose core is constrained to have one or more core clock signal frequencies no lower than a predetermined multiple of a lowest of one or more bus clock signal frequencies for one or more clock signals of said bus,

wherein said processor is able, in a power-save mode of said apparatus, to generate one or more bus clock signals whose lowest frequency is lower than a lowest frequency of said one or more bus clock signals in a performance mode of said apparatus.

22. The apparatus of claim 21, wherein said processor further comprises:

a phase locked loop to generate an intermediate clock signal from a system clock signal of said processing system, said phase locked loop including one or more digital frequency dividers to divide said intermediate clock signal in order to generate said one or more bus clock signals.

23. The apparatus of claim 22, wherein said phase locked loop further comprises one or more additional digital frequency dividers to divide said intermediate clock signal in order to generate one or more core clock signals for said core.

24. The apparatus of claim 22, wherein said processor further comprises:

another phase locked loop to generate one or more core clock signals for said core from said system clock signal.

25. The apparatus of claim 21, wherein said processing system further comprises:

a bus interface to receive said one or more bus clock signals.

26. The apparatus of claim 25, further comprising:

a power supply unit to supply a lower voltage to said bus interface than that which supports said performance mode.