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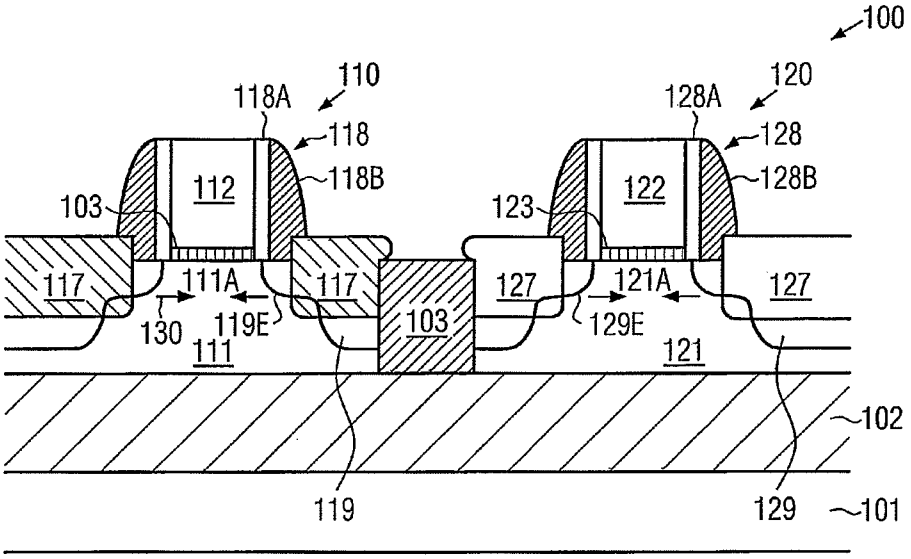
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(54) Title: TECHNIQUE FOR FORMING RECESSED STRAINED DRAIN/SOURCE IN NMOS AND PMOS TRANSISTORS



(57) Abstract: By forming a strained semiconductor layer (117, 217) in a PMOS transistor (110, 210), a corresponding compressively strained channel region (11 IA) may be achieved, while, on the other hand, a corresponding strain in the NMOS transistor (120, 220) may be relaxed. Due to the reduced junction resistance caused by the reduced band gap of silicon/germanium in the NMOS transistor (120, 220), an overall performance gain is accomplished, wherein, particularly in partially depleted SOI devices, the deleterious floating body effect is also reduced, due to the increased leakage currents generated by the silicon/germanium layer (117, 127, 217, 227) in the PMOS (110, 210) and NMOS transistor (120, 220).

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