CLAIMS

1. A method of designing an integrated circuit with finfet based logic cells, the method comprising forming at least a first logic cell with at least one of: two or more p-diffusion regions, stacked in a y-direction, with each of the two or more p-diffusion regions comprising two or more fins in an x-direction, and each of the two or more p-diffusion regions comprising an island with p-type doping in an n-type well; or two or more n-diffusion regions, stacked in the y-direction, with each of the two or more n-diffusion regions comprising two or more fins in the x-direction, and each of the two or more n-diffusion regions comprising an island with n-type doping in a p-type well.

2. The method of claim 1, further comprising forming the first logic cell with at least one of: a first p-diffusion region and a second p-diffusion region, the first p-diffusion region and the second p-diffusion region having different fin counts; or a first n-diffusion region and a second n-diffusion region, the first n-diffusion region and the second n-diffusion region having different fin counts.

3. The method of claim 1, further comprising forming a distributed power rail network with at least one of: at least a first local power rail associated with at least one of the two or more p-diffusion regions; or at least a second local power rail associated with at least one of the two or more n-diffusion regions.

4. The method of claim 3, wherein, at least one of: the first local power rail is dedicated to the at least one of the two or more p-diffusion regions; or the second local power rail is dedicated to the at least one of the two or more n-diffusion regions.

5. The method of claim 1, further comprising forming the first logic cell with at least one of: a first p-diffusion region and a second p-diffusion region, the first p-diffusion region and the second p-diffusion region formed with different levels of p-type implants; or a first n-diffusion region and a second n-diffusion region, the first n-diffusion region and the second n-diffusion region formed with different levels of n-type implants.

6. The method of claim 1, further comprising forming the first logic cell with at least one of: a first pfet formed in a first p-diffusion region and a second pfet formed in a second p-diffusion region, the first pfet and the second pfet having different threshold voltages or channel lengths; or a first nfet formed in a first n-diffusion region and a second nfet formed in a second n-

diffusion region, the first nfet and the second nfet having different threshold voltages or channel lengths.

7. The method of claim 1, comprising forming the first logic cell as a 2-input NAND gate with a ratio logic wherein a first fin count is different from a second fin count.

8. The method of claim 7, further comprising forming two pfets having the first fin count equal to two fins in the first p-diffusion region and connecting the two pfets connected in parallel; and forming two nfets, with each of the two nfets having the second fin count equal to four fins, with two of the four fins in the first n-diffusion region and two of the four fins in another n-diffusion region and connecting the two nfets in series.

9. The method of claim 8, further comprising forming at least one poly line, the at least one poly line shared between the two pfets and the two nfets.

10. The method of claim 9, further comprising placing a poly cut on the at least one poly line between the first p-diffusion region and another p-diffusion of the first logic cell.

11. The method of claim 9, further comprising forming at least one gate via on the at least one poly line between the two pfets and the two nfets and connecting a metal to diffusion (MD) layer to the at least one gate via.

12. A method of designing an integrated circuit with finfet based logic cells, the method comprising: placing a first logic cell having a first logic cell boundary adjacent to a second logic cell having a second logic cell boundary, wherein the first logic cell boundary and the second logic cell boundary have a common edge, wherein the first logic cell comprises at least one pfet formed on a first p-diffusion region with a first fin count and at least one nfet formed on a first n-diffusion region with a second fin count, and wherein the second logic cell comprises at least one pfet formed on a second p-diffusion region with the first fin count and at least one nfet formed on a second n-diffusion region with the second fin count; and forming at least one of: a first p-diffusion fill traversing the common edge and joining the first p-diffusion region of the first logic cell and the second p-diffusion region of the second logic cell; or a first n-diffusion fill traversing the common edge and joining the first n-diffusion region of the first logic cell and the second n-diffusion region of the second logic cell.

13. The method of claim 12, comprising extending a length of diffusion (LOD) of at least one of: the first p-diffusion region of the first logic cell and the second p-diffusion region of the second logic cell with the first p-diffusion fill; or the first n-diffusion region of the first logic cell and the second n-diffusion region of the second logic cell with the first n-diffusion fill.

14. The method of claim 12, wherein at least one of: the first p-diffusion region of the first logic cell and the second p-diffusion region of the second logic cell are of a common first potential; or the first n-diffusion region of the first logic cell and the second n-diffusion region of the second logic cell are of a common second potential.

15. The method of claim 14, further comprising forming at least one of: a connection between the first p-diffusion fill and a first metal layer at the common first potential; or a connection between the first n-diffusion fill and a second metal layer at the common second potential.

16. The method of claim 15, wherein the common first potential corresponds to a potential of a power rail, and the common second potential corresponds to a potential of a ground rail or a local interconnect.

17. The method of claim 16, wherein at least one of the power rail or the ground rail are distributed in a space between the diffusion regions of the first logic cell and the second logic cell.

18. The method of claim 12, further comprising floating at least one poly line of the first logic cell or the second logic cell, the at least one poly line adjacent to the common edge and intersecting at least one of the first p-diffusion region, the second p-diffusion region, the first n-diffusion region, or the second n-diffusion region.

19. The method of claim 12, wherein the first fin count is different from the second fin count.

20. The method of claim 19, wherein the first logic cell is a 2-input NAND gate with a ratio logic between the first fin count and the second fin count.

21. The method of claim 20, wherein forming the 2-input NAND gate comprises connecting two pfets in parallel, with each of the two pfets having the first fin count equal to two fins formed on

the first p-diffusion region; and connecting two nfets in series, with each of the two nfets having the second fin count equal to four fins, with two of the four fins formed on the first n-diffusion region and two of the four fins formed on another n-diffusion region of the first logic cell connected in series with the first n-diffusion region.

22. The method of claim 21, comprising sharing at least one poly line between the two pfets and the two nfets.

23. The method of claim 21, comprising forming at least one gate via on at least one poly line between the two pfets and the two nfets.

24. The method of claim 23, comprising connecting the at least one gate via to a metal to diffusion (MD) layer.

25. The method of claim 24, wherein the second logic cell is an inverter comprising two pfets, with each pfet having the first fin count equal to two fins and formed in two p-diffusion regions including at least the second p-diffusion region; and two nfets, with nfet each having the second fin count equal to two fins and formed in two n-diffusion regions including at least the second n-diffusion region.

26. The method of claim 20, comprising placing a poly cut on at least one poly line between the first p-diffusion region and another p-diffusion of the first logic cell.

27. The method of claim 12, further comprising tailoring implants or threshold voltages of at least one of the first or second n-diffusion regions or first or second p-diffusion regions.

28. The method of claim 12, further comprising tailoring channel lengths of gates formed in at least one of the first or second n-diffusion regions or first or second p-diffusion regions.

29. A method of designing an integrated circuit with finfet based logic cells, the method comprising: forming a first full row comprising at least a first full-row height logic cell, wherein the first full-row height logic cell comprises at least one of two or more p-diffusion regions or two or more n-diffusion regions; forming a second full row adjacent to the first full row, the second full row comprising at least a second full-row height logic cell, wherein the second full-

row height logic cell comprises at least one of two or more p-diffusion regions or two or more n-diffusion regions; wherein the two or more p-diffusion regions of the first full row and the second full row are stacked in a y-direction, with each of the two or more p-diffusion regions comprising two or more fins in an x-direction, and each of the two or more p-diffusion regions comprising an island with p-type doping in an n-type well; or wherein the two or more n-diffusion regions of the first full row and the second full row are stacked in the y-direction, with each of the two or more n-diffusion regions comprising two or more fins in the x-direction, and each of the two or more n-diffusion regions comprising an island with n-type doping in a p-type well; and interspersing one or more sub-rows between the first full row and the second full row, wherein at least a first sub-row of the one or more sub-rows comprises a first half-row height logic cell comprising at least one p-diffusion region and at least one n-diffusion region, wherein at least one of: the at least one p-diffusion region of the first half-row height logic cell is adjacent to one of the two or more p-diffusion regions of the first full-row height logic cell or the second full-row height logic cell, or the at least one n-diffusion region of the first half-row height logic cell is adjacent to one of the two or more n-diffusion regions of the first full-row height logic cell or the second full-row height logic cell.

30. The method of claim 29, comprising forming the second full-row height logic cell without vertically mirror-flipping the second full-row height logic cell with respect to the first full-row height logic cell.

31. The method of claim 29, comprising forming adjacent half-row height cells of two adjacent sub-rows of the one or more sub-rows by vertically mirror-flipping the adjacent half-row height cells of the two adjacent sub-rows of the one or more sub-rows with respect to one another.

32. The method of claim 29, further comprising extending, with at least one p-diffusion fill, a length of diffusion of the at least one p-diffusion region of the first half-row height logic cell and one of the two or more p-diffusion regions of the first full-row height logic cell or the second full-row height logic cell.

33. The method of claim 29, further comprising extending, with at least one n-diffusion fill, a length of diffusion of the at least one n-diffusion region of the first half-row height logic cell and one of the two or more n-diffusion regions of the first full-row height logic cell or the second full-row height logic cell.

34. A non-transitory computer-readable storage medium comprising code, which, when executed by a processor, causes the processor to perform operations for designing an integrated circuit with finfet based logic cells, the non-transitory computer-readable storage medium comprising:

code for forming at least a first logic cell with at least one of: two or more p-diffusion regions, stacked in a y-direction, with each of the two or more p-diffusion regions comprising two or more fins in an x-direction, and each of the two or more p-diffusion regions comprising an island with p-type doping in an n-type well; or two or more n-diffusion regions, stacked in the y-direction, with each of the two or more n-diffusion regions comprising two or more fins in the x-direction, and each of the two or more n-diffusion regions comprising an island with n-type doping in a p-type well.

35. A non-transitory computer-readable storage medium comprising code, which, when executed by a processor, causes the processor to perform operations for designing an integrated circuit with finfet based logic cells, the non-transitory computer-readable storage medium comprising: code for placing a first logic cell having a first logic cell boundary adjacent to a second logic cell having a second logic cell boundary, wherein the first logic cell boundary and the second logic cell boundary have a common edge, wherein the first logic cell comprises at least one pfet formed on a first p-diffusion region with a first fin count and at least one nfet formed on a first n-diffusion region with a second fin count, and wherein the second logic cell comprises at least one pfet formed on a second p-diffusion region with the first fin count and at least one nfet formed on a second n-diffusion region with the second fin count; and code for forming at least one of: a first p-diffusion fill traversing the common edge and joining the first p-diffusion region of the first logic cell and the second p-diffusion region of the second logic cell; or a first n-diffusion fill traversing the common edge and joining the first n-diffusion region of the first logic cell and the second n-diffusion region of the second logic cell.

36. A non-transitory computer-readable storage medium comprising code, which, when executed by a processor, causes the processor to perform operations for designing an integrated circuit with finfet based logic cells, the non-transitory computer-readable storage medium comprising: code for forming a first full row comprising at least a first full-row height logic cell, wherein the first full-row height logic cell comprises at least one of two or more p-diffusion regions or two or more n-diffusion regions; code for forming a second full row adjacent to the first full row, the second full row comprising at least a second full-row height logic cell, wherein the second full-row height logic cell comprises at least one of two or more p-diffusion regions or two or more n-diffusion regions; wherein the two or more p-diffusion regions of the first full row and the second full row are stacked in a y-direction, with each of the two or more p-diffusion regions comprising two or more fins in an x-direction, and each of the two or more p-diffusion regions comprising an island with p-type doping in an n-type well; or wherein the two or more n-diffusion regions of the first full row and the second full row are stacked in the y-direction, with each of the two or more n-diffusion regions comprising two or more fins in the x-direction, and each of the two or more n-diffusion regions comprising an island with n-type doping in a p-type well; and code for interspersing one or more sub-rows between the first full row and the second full row, wherein at least a first sub-row of the one or more sub-rows comprises a first half-row height logic cell comprising at least one p-diffusion region and at least one n-diffusion region,

wherein at least one of: the at least one p-diffusion region of the first half-row height logic cell is adjacent to one of the two or more p-diffusion regions of the first full-row height logic cell or the second full-row height logic cell, or the at least one n-diffusion region of the first half-row height logic cell is adjacent to one of the two or more n-diffusion regions of the first full-row height logic cell or the second full-row height logic cell.