

ABSTRACT

DUAL CHAMBER PLASMA ETCHER WITH ION ACCELERATOR

[0110] The embodiments herein generally deal with semiconductor processing methods and apparatus. More specifically, the embodiments relate to methods and apparatus for etching a semiconductor substrate. A partially fabricated semiconductor substrate is provided in a reaction chamber. The reaction chamber is divided into an upper sub-chamber and a lower sub-chamber by a grid assembly. Plasma is generated in the upper sub-chamber, and the substrate is positioned in the lower sub-chamber. The grid assembly includes at least two grids, each of which is negatively biased, and each of which includes perforations which allow certain species to pass through. The uppermost grid is negatively biased in order to repel electrons. The lowermost grid is biased further negative (compared to the uppermost grid) in order to accelerate positive ions from the upper to the lower sub-chamber. Etching gas is supplied directly to the lower sub-chamber. The etching gas and ions react with the surface of the substrate to etch the substrate as desired.

Fig. 2