

STRUCTURE FOR RADIOFREQUENCY APPLICATIONS

FIELD OF THE INVENTION

The present invention relates to the field of integrated radiofrequency devices

5 TECHNOLOGICAL BACKGROUND OF THE INVENTION

Integrated devices are usually produced on substrates in the form of wafers, which mainly serve as a medium for their manufacture. However, the rise in the level of integration and in the performances expected of these devices results in an
10 ever increasing linkage between their performances and the characteristics of the substrate on which they are formed. This is particularly the case of radiofrequency (RF) devices processing signals with a frequency of between approximately 3kHz and 300GHz, which are more particularly applied in the
15 telecommunications field (cellular telephony, Wi-Fi, Bluetooth...).

By way of an example of device/substrate coupling, the electromagnetic fields, originating from the high-frequency signals propagating through the devices, penetrate deeply into
20 the substrate where they interact with any charge carriers located there. This results in problems of non-linear distortion of the signal (harmonics), unnecessary consumption of a portion of the energy of the signal by insertion loss and possible influences among components.

25 Hence, RF devices display characteristics governed both by their architectures and production processes and by the ability of the substrate on which they are manufactured to limit insertion losses, diaphonies between neighbouring devices and phenomena of non-linear distortion generating
30 harmonics.

With the explosion of the demand for data, created by "multimedia" applications, changes in mobile telephony standards (2G, 3G, LTE, LTE-A...) likewise impose increasingly stringent specifications on RF components. The RF performances
5 of these components typically need to be guaranteed between -20°C and +120°C, implying that the electrical properties of the substrate are stable within this temperature range.

Radiofrequency devices, such as switches and antenna adapters in addition to power amplifiers, can be produced on
10 different types of substrate.

Silicon on sapphire substrates, commonly referred to as SOS, are known in which the components, produced using microelectronic technologies in the superficial layer of silicon, benefit from the insulating properties of the
15 sapphire substrate, which are temperature-independent. For example, antenna switches and power amplifiers manufactured on this type of substrate display very good merit factors, but are mainly used for niche applications owing to the overall cost of the solution.

20 Substrates based on high-resistivity silicon are also known, comprising a supporting substrate, a trapping layer arranged in the supporting substrate, a dielectric layer arranged on the trapping layer and a semiconducting layer arranged on the dielectric layer. The supporting substrate
25 usually has a resistivity greater than 1 kOhm.cm. The trapping layer may comprise undoped polycrystalline silicon. The combination of a high-resistivity supporting substrate and a trapping layer according to the state of the art makes it possible to reduce the device/substrate coupling mentioned
30 above, thereby ensuring good performances of the RF devices. In this respect, the persons skilled in the art will find a review of the performances of RF devices manufactured on the high-resistivity semiconducting substrate known in the prior

art in "Silicon-on-insulator (SOI) Technology, manufacture and applications", points 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, from Woodhead Publishing.

5 Nevertheless, these substrates fail to fulfil the most stringent specifications: for example, when localised heating beyond approximately 80°C occurs, the resistivity of these substrates declines owing to generation of heat carriers in the substrate and device/substrate coupling once again becomes a major contributor to attenuation and distortion of the
10 signal and interference among components. Deteriorations in performance are also observed when the temperature falls to below 0°C.

AIM OF THE INVENTION

15 An aim of the invention therefore consists in providing a suitable structure for radiofrequency applications, solving the drawbacks of the prior art. An aim of the invention is to provide an integrated structure delivering radiofrequency performances, particularly with the range of temperatures of use.

20 BRIEF DESCRIPTION OF THE INVENTION

The invention concerns a structure for radiofrequency applications comprising:

- a semiconducting supporting substrate;
- a trapping layer arranged on the supporting substrate.

25 According to the invention, the trapping layer is remarkable in that it comprises a defect density greater than a predetermined defect density; the predetermined defect density is the defect density for which the electrical

resistivity of the trapping layer is greater than or equal to 10kohm.cm over a temperature range [-20 °C; +120°C].

The structure for radiofrequency applications according to the invention therefore displays temperature-stable
5 electrical properties, ensuring good stability and repeatability of the RF performances within the range of temperatures of use.

According to advantageous characteristics of the invention, taken either separately or in combination:

10 - the trapping layer has a resistivity at 20°C greater than 10 kOhm.cm and preferably greater than 50 kOhm.cm;

 - the difference in the thermal expansion coefficient between the trapping layer and the supporting substrate is less than 5 ppm/k between 100°C and 1200°C;

15 - the trapping layer comprises microstructures of a size smaller than 20 nm and preferably smaller than 10 nm;

 - the trapping layer comprises a porous or polycrystalline material;

 - the trapping layer comprises polycrystalline silicon
20 containing 1 to 20% of carbon;

 - the thickness of the trapping layer is between 10 and 50 μm and preferably between 20 and 30 μm ;

 - the supporting substrate comprises at least one of the materials selected from the following group: silicon, silicon
25 germanium and silicon carbide;

 - the resistivity of the supporting substrate is between 10 and 2000 Ohm.cm.

According to other advantageous characteristics of the invention, taken either separately or in combination:

- an active layer is arranged on the trapping layer;
- the active layer is transferred to the trapping layer
5 by direct bonding;
- the active layer is formed from a semiconducting material;
- the active layer is formed from a piezoelectric material;
- 10 - the thickness of the active layer is included between 10 and 50 μm ;
- a dielectric layer is arranged between the trapping layer and the active layer;
- the dielectric layer is transferred to the trapping
15 layer by direct bonding;
- the dielectric layer is between 10 nm and 6 μm .

According to other advantageous characteristics of the invention, taken alone or in combination, at least one microelectronic device is present on or in the active layer;

- 20 - the microelectronic device is a switching circuit or an antenna adaptation circuit or even a radiofrequency amplification circuit;
- the microelectronic device comprises a plurality of active components and a plurality of passive components;
- 25 - the microelectronic device comprises at least one control element and one MEMS switching element consisting of an ohmic-contact microswitch and a capacitive microswitch;

- the microelectronic device is a radiofrequency filter operating by volume or surface sound wave propagation.

BRIEF DESCRIPTION OF THE DRAWINGS

Further characteristics and advantages of the invention will be clear from the following detailed description of the invention, made in reference to the appended figures, in which:

- figure 1 represents a structure for radiofrequency applications according to the invention, comprising a substrate and a trapping layer;

- figure 2 shows comparative curves of the resistivity of structures according to the state of the art and a structure according to the invention;

- figures 3a and 3b respectively represent a structure for radiofrequency applications according to the invention, furthermore comprising an active layer;

- figures 4a and 4b respectively represent a structure for radiofrequency applications according to the invention, furthermore comprising a microelectronic device.

DETAILED DESCRIPTION OF THE INVENTION

La structure 1,1', 11 for radiofrequency applications according to the invention comprises a semiconducting supporting substrate 2. The supporting substrate 2 may be made of materials commonly used in the microelectronic, optical, optoelectronic and photovoltaic industry. In particular, the supporting substrate 2 may comprise at least one material selected from the following group: silicon, silicon germanium and silicon carbide, etc. The resistivity of the supporting

substrate may be between 1 and 10,000 ohm.cm; it is advantageously between 10 and 2000 ohm.cm.

The structure 1,1',11 for radiofrequency applications also comprises a trapping layer 3 arranged on the supporting substrate 2, as illustrated in figures 1, 3 and 4. The trapping layer comprises a defect density greater than a predetermined defect density; the predetermined defect density is the defect density for which the electrical resistivity of the trapping layer is greater than or equal to 10kohm.cm over the temperature range $[-20^{\circ}\text{C}; +120^{\circ}\text{C}]$.

The number of defects or the defect density may be determined using different methods including transmission electron microscopy (TEM). The defect density thus being known, the electrical resistivity of the trapping layer 3 can be measured at different temperatures. By way of example, the predetermined defect density may be between 10^{19} and 10^{21} cm^{-3} (for example, in the case of a trapping layer made of polycrystalline silicon).

In the case of an adequate defect density in the trapping layer 3 (said predetermined defect density according to the invention) correlated with a high resistivity, the conductivity mechanism in the layer 3 is dominated by a hopping conductivity regime. This makes it possible to maintain a resistivity level above the threshold of 10kohm.cm, within the temperature range $[-20^{\circ}\text{C}; +120^{\circ}\text{C}]$. The person skilled in the art will encounter a presentation of hopping electrical conductivity in the document "N.F.Mott, Phil. Mag, 19, 835, 1969".

"Defect", without wishing to be restrictive, means grain boundaries in polycrystalline materials, empty areas in porous materials, gaps, inclusions...

Advantageously, the trapping layer 3 comprises microstructures of a size smaller than 20 nm; preferably, the microstructures even have a size smaller than 10 nm. "Microstructures" mean crystallites, particularly for polycrystalline materials, also referred to as grains.

Thus, the smaller the microstructures in the trapping layer 3, the greater the defect density in the latter may be.

Advantageously, the trapping layer 3 also has a resistivity greater than 10 kohm.cm, at ambient temperature; preferentially, it has a resistivity of more than 50 kohm.cm.

The aforementioned physical characteristics (microstructure) and electrical characteristics (resistivity) of the trapping layer 3 guarantee a hopping conductivity mechanism in the latter, displaying a low level of temperature dependence; the resistivity of the trapping layer 3 likewise displays low temperature dependence compared with state of the art layers, maintaining a level of more than 10 kohm.cm over the entire intended temperature range.

The thickness of the trapping layer 3 may be between 10 and 50 nm; preferably, it is between 20 and 30 nm. The thickness of the trapping layer 3 is such that the RF signals originating from the components manufactured on the structure 1,1' penetrate and are propagated predominately in the trapping layer 3, without reaching the underlying supporting substrate 2. The electrical properties of the supporting substrate 2 and trapping layer 3 assembly are thus essentially dictated by the properties of the trapping layer 3. Consequently, there are fewer requirements imposed on the resistivity of the supporting substrate 2. In the case of silicon substrates, the cost and availability of substrates with a resistivity within the range of 10-1000ohm.cm are more

favourable than those of substrates with a very high resistivity ($>1000\text{ohm.cm}$ and up to 20kohm.cm).

The trapping layer 3 also has a small difference in thermal expansion coefficient in relation to the supporting substrate 2 between 100°C and 1200°C and advantageously less than 5 ppm/K . Indeed, subsequent manufacture of RF components on top of the trapping layer 3 generally requires heat treatment stages at temperatures exceeding 850°C , or even exceeding 1100°C , for example 1200°C . At such temperatures and for thicknesses of the trapping layer 3 on the order of a few tens of microns, an excessive difference in thermal expansion coefficient between the trapping layer 3 and the supporting substrate 2 may cause deformations that are incompatible with subsequent manufacturing processes or even liable to break the substrate. A difference in thermal expansion coefficient between the trapping layer 3 and the supporting substrate 2 of less than 5 ppm/K avoids risks of breakage of the structure.

The trapping layer 3 advantageously consists of porous or polycrystalline material. According to a first, non-restrictive example, the supporting substrate 2 is a silicon substrate and the trapping layer 3 is a porous silicon layer comprises microstructures of a size smaller than 20 nm , having a porosity greater than 50% and a thickness of 30 nm . Formation of the porous silicon layer advantageously comprises the following stages:

- formation of a layer of doped silicon p (boron for example) by epitaxy on the supporting substrate, wherein said formation is performed by means of a vapour deposition method, at temperature of between 900°C and 1200°C , with trichlorosilane and diborane (B_2H_6) as precursors;

- subsequently, electrochemical anodizing.

The size of the microstructures gives the trapping layer 3 a resistivity of more than 10k Ω .cm, stable over the entire temperature range [-20°C; 120°C]. The pores of the trapping layer 3 are not affected during a high temperature heat treatment stage (typically up to 1100°C): since the size of the grains in the layer 3 governs the resistivity of said layer 3, its electrical properties remain unchanged after heat treatments for production of the components.

According to a second, non-restrictive example, the supporting substrate 2 is a silicon substrate and the trapping layer 3 is a polycrystalline silicon layer comprises grains of a size smaller than 20 nm, preferably smaller than 10 nm and having a thickness of between 10 and 50 μ m, for example 30 μ m. The difference in thermal expansion coefficient between the supporting substrate 2 and the trapping layer 3 is less than 5 ppm/K and prevents any excessive deformation of the substrate capable of causing its breakage. The trapping layer 3 furthermore has a resistivity of more than 50k Ω .cm ambient temperature.

In order to allow the trapping layer 3 to maintain its physical characteristics (microstructures) following application of high-temperature heat treatments (required for subsequent manufacture of RF components), the polycrystalline silicon layer advantageously includes carbon at a content of between 1 and 20%, for example 5%. Creation of such a trapping layer 3 requires use of vapour-phase chemical deposition methods. The layer formation temperature must in this case be greater than 700°C, preferably greater than 900°C and even more preferentially between 1100 and 1200°C. The Carbone (C) precursors may comprise at least one of the elements selected from among: methylsilane (SiH_3CH_3), methane (CH_4), ethane (C_2H_6), propane (C_3H_8), butane (C_4H_{10}) and methyltrichlorosilane (SiCH_3Cl_3). The Silicon (Si) precursors

may comprise at least one of the elements selected from among: silane (SiH_4), disilane (Si_2H_6), dichlorosilane (SiH_2Cl_2), trichlorosilane (SiHCl_3) and tetrachlorosilane (SiCl_4).

Carbon doping of the polysilicon layer allows
 5 stabilisation of the grain size during thermal annealing comprising a temperature increase greater than 850°C , for example 1200°C . Indeed, without this carbon doping, the grains of the polysilicon trapping layer 3 are reorganised and undergo an increase in size; this results in a drastic
 10 reduction in the resistivity of the trapping layer 3 and deterioration in its electrical characteristics.

When carbon doping is introduced into the polysilicon trapping layer 3, the carbon atoms are concentrated at the grain boundaries and freeze any reorganisation of the grains
 15 during thermal annealing comprising a temperature increase of more than 850°C . Consequently, the thermal treatment stages for production of the components do not affect the physical and electrical properties of the trapping layer 3.

Figure 2 illustrates the resistivity of the trapping
 20 layer 3 according to the invention (curve C) simulated over the temperature range [20°C - 140°C]: it will be noted that the resistivity of said layer 3 is greater than $10\text{k}\Omega\cdot\text{cm}$, at least up to 120°C , corresponding to the upper bound of the intended temperature range. In comparison, the simulated
 25 resistivity of state of the art structures (curves A and B) shows values much lower than $10\text{k}\Omega\cdot\text{cm}$ at 120°C , which does not allow RF performances sufficient to fulfil the stringent specifications of the LTE (Long Term Evolution) standards of mobile telephony. A structure 1,1', 11 for RF applications
 30 according to the invention will, for its part, guarantee a stable performance that is insensitive to temperature variations within the range of use.

According to a first embodiment of the invention, the structure 1 for radiofrequency applications may adopt the form of a wafer with dimensions compatible with microelectronic processes, for example of a diameter of 200 mm or 300 mm, comprising the supporting substrate 2 and the trapping layer 3. The latter may be produced according to the first or second example mentioned above, though these manufacturing examples are nevertheless not exhaustive.

According to a second embodiment of the invention, illustrated in figure 3a, the structure for radiofrequency applications may adopt the form of a wafer and furthermore comprise an active layer 5, arranged on the trapping layer 3, in and on which it will be possible to produce RF components. The active layer 5 may advantageously consist of semiconductive materials and/or piezoelectric materials. Advantageously, without its being however restrictive, the active layer 5 comprises at least one of the materials from among: silicon, silicon carbide, silicon germanium, lithium niobate, lithium tantalate, quartz and aluminium nitride. The thickness of the active layer 5 may vary between a few nanometres (10 nm for example) and several tens of microns (50 mm for example) according to the components to be manufactured.

By way of example, the active layer 5 is transferred to a supporting substrate 2 comprising the trapping layer 3, using one of the methods of transferring thin layers well known to the person skilled in the art, wherein:

the Smart Cut™ method, based on an implantation of light ions of hydrogen and/or helium in a donor substrate and bonding for example by molecular adhesion of this donor substrate to the trapping layer 3, arranged in turn on the supporting substrate 2; a detachment stage subsequently allows separation of a superficial fine layer of the donor substrate

(the active layer), at the level of the fragilization plane defined by the ion implantation depth. Finishing stages that may include high temperature heat treatments finally give the active layer 5 the required crystalline and surface quality.

5 This method is particularly suitable for manufacturing thin active layers between a few nanometres and approximately 1.5 mm thick, for silicon layers for example.

- the Smart Cut method followed by an epitaxy stage, making it possible in particular to obtain thicker active
10 layers, for example between a few tens of nm and 20 mm thick.

- direct bonding as well as mechanical, chemical and/or chemical mechanical methods; they involve assembling a donor substrate by molecular adhesion on the trapping layer 3, arranged in turn on the supporting substrate 2 and
15 subsequently thinning the donor substrate down to the desired active layer thickness, by grinding for example and by CMP (chemical mechanical polishing). These methods are particularly suitable for transferring thick layers, between a few microns and several tens of microns for example and up to
20 a few hundreds of microns.

According to a variant of the second embodiment, illustrated in figure 3b, the structure 1' for radiofrequency applications may also comprise a dielectric layer 4, arranged between the active layer 5 and the trapping layer 3.
25 Advantageously, without its being restrictive however, the dielectric layer 4 will comprise at least one of the materials from among: silicon dioxide, silicon nitride and aluminium oxide... Its thickness may vary between 10 nm and 6 mm.

The dielectric layer 4 is obtained by thermal oxidation
30 or by deposition of LPCVD or PECVD or HPD on the trapping layer 3 or on the donor substrate prior to transferring the active layer 5 to the trapping layer 3.

According to a third embodiment, illustrated in figure 4a, the structure 11 for radiofrequency applications may also comprise or consist of a microelectronic device 6 on or in the active layer 5, wherein the latter is arranged on a dielectric layer 4 or directly on the trapping layer 3. The microelectronic device 6 may be a switching circuit, an adaptation or tuner circuit or even a power amplifier circuit, produced using silicon microelectronics technologies. The silicon active layer 5 typically has a thickness of between 50 nm and 180 nm, for example 145 nm and the underlying dielectric layer 4 has a thickness of between 50 nm and 400 nm, for example 200 nm; the trapping layer 3 is arranged between the dielectric layer 4 and the supporting substrate 2. The microelectronic device 6 produced in and on the active layer 5 comprises a plurality of active components (of the MOS, bipolar type...) and a plurality of passive components (of the capacitance, inductance, resistor, resonator and filter type...). Manufacture of the microelectronic components requires carrying out several stages including heat treatments at high temperatures, typically at 950-1100°C or indeed above. The trapping layers 3 described in the first and second examples previously mentioned retain their physical and electrical properties after such heat treatments.

In a variant of this embodiment, the microelectronic device 6 can be initially produced on an SOI (silicon on insulator)-type substrate and subsequently be transferred using a layer transfer method known to a person skilled in the art to a structure 1 according to the invention comprising a trapping layer 3 arranged on the supporting substrate 2. In this case, as illustrated in figure 4b, the structure 11 comprises a supporting substrate 2 on which the trapping layer 3 is arranged; the layer of components of the microelectronic device 6 appears on top of the latter: the so-called "back end" of metallic interconnection layers and of dielectrics is

arranged on top of the trapping layer 3, with the so-called "front end" (silicon), partly produced in the active layer, being itself on top of the "back end" part. Finally, the active layer 5 and optionally a dielectric layer 4' is
5 furthermore located on top.

In both sets of circumstances, the electromagnetic fields, derived from the high frequency signals intended to be propagated in the devices 6 and which will penetrate into the trapping layer 3, will only suffer minor losses (insertion
10 losses) and interferences (diaphony, harmonics) owing to the resistivity greater than 10 kohm.cm of the trapping layer 3 and moreover throughout the entire range of temperature of use [-20°C; 120°C].

According to a fourth embodiment, the structure 11 for
15 radiofrequency applications may comprise or consist of a microelectronic device 6 featuring at least one control element and a MEMS (microelectromechanical systems) switching element consisting of an ohmic-contact microswitch and a capacitive microswitch.

20 Manufacture of the MEMS can be facilitated by the presence of a dielectric layer 4 under an active layer 5 of silicon. The structure 11 according to the invention may therefore comprise, by way of example, an active layer 5 made of silicon of a thickness of between 20 nm and 2000 nm,
25 advantageously 145 nm, in addition to an underlying dielectric layer 4 of a thickness of between 20 nm and 1000 nm, advantageously 400 nm; the trapping layer 3 is arranged between the dielectric layer 4 and the supporting substrate 2. Manufacture of the MEMS part is subsequently based on surface
30 micromachining methods, permitting in particular release of beams or movable membranes in the active layer 5 of silicon.

Alternately and as well known to persons skilled in the art, the MEMS part can be produced directly on the trapping layer 3, by successive deposition of a plurality of layers (including an electrode, a dielectric, a sacrificial layer and an active layer) and by creating motifs on these different layers.

The microelectronic methods used to manufacture the control element(s) (CMOS for example), usually performed before the MEMS part, require, as in the previous embodiment, application of heat treatments at high temperatures. The fact that the trapping layer 3 according to the invention does not undergo any physical and electrical changes during this type of treatment is highly advantageous.

In the same manner as for the third embodiment, the high frequency signals that are propagated in this device generate electromagnetic fields that penetrate into the trapping layer 3. The losses (insertion losses), distortions (harmonics) and other interferences (diaphony,...) will be less owing to the higher resistivity at 10 kohm.cm of the trapping layer 3 throughout the entire intended temperature range for use of the device 6.

According to a fifth embodiment, the structure 11 for radiofrequency applications may comprise or consist of a microelectronic device 6 featuring a radiofrequency filter operating by volume sound wave propagation (referred to as BAW [Bulk Acoustic Wave]).

Manufacture of a BAW filter of the FBAR (thin-Film Bulk Acoustic Resonator) type requires an active layer 5 formed of a piezoelectric material, in which the sound wave will be confined, between the two surrounding electrodes. The structure 11 according to the invention may therefore comprise, by way of example, an active layer 5 made of

aluminium nitride of a thickness of between 50 nm and 1 mm, advantageously 100 nm, in addition to a dielectric layer 4 (for example consisting of silicon oxide) the thickness of which is between 1 and 6 mm; the trapping layer 3 is arranged
5 between the dielectric layer 4 and the supporting substrate 2. Insulating cavities are arranged under the active areas of the filter, i.e. the areas in which the sound waves will propagate.

Manufacture of the BAW filter furthermore requires stages
10 involving depositing electrodes to which the RF signal will be applied.

The structure according to the invention makes it possible on the one hand to restrict the depth of the insulating cavities, the insulating function of which in
15 relation to the substrate is rendered less critical by the resistivity greater than 10 kohm.cm of the trapping layer 3, throughout the entire intended temperature range; this is an advantage in terms of simplification, flexibility and robustness of the manufacturing process of these devices.
20 Furthermore, the structure 11 according to the invention makes it possible to obtain better performances of the filters throughout the entire intended temperature range for use of the device 6, particularly in terms of linearity.

In a variant of this fifth embodiment, the
25 microelectronic device 6 comprises a radiofrequency filter operating by surface sound wave propagation (referred to as SAW [Surface Acoustic Wave]).

Manufacture of an SAW filter requires an active layer 5 formed of a piezoelectric material, on the surface of which a
30 comb-like array of electrodes will be produced: the sound wave is intended to propagate between these electrodes. The structure 11 according to the invention may therefore

comprise, by way of example, an active layer 5 made of lithium tantalate of a thickness of between 200 nm and 20 mm, advantageously 0.6 mm; the trapping layer 3 is arranged between the active layer 5 and the supporting substrate 2. A dielectric layer 4 may optionally be added between the active layer 5 and the trapping layer 3.

The structure 11 according to the invention makes it possible to obtain better filter performances throughout the entire intended temperature range for use of the device 6, particularly in terms of insertion losses and linearity.

The structures 1,1', 11 for radiofrequency applications according to the invention are not limited to the embodiments mentioned above. They are suitable for any application in which high frequency signals propagate and are liable to undergo undesirable losses or interferences in a supporting substrate 2, since the physical and electrical characteristics of the trapping layer 3 arranged on the supporting substrate 2 give the structure 1,1', 11 good RF properties (restricting losses, non-linearities and other interferences), stable within a range of temperatures of use, i.e. [-20°C; 120°C].

CLAIMS

1. Structure (I,I',II) for radiofrequency applications, comprising:

- a semiconducting supporting substrate (2);

5 • a trapping layer (3) arranged on the supporting substrate (2);

wherein the trapping layer (3) is characterised in that it comprises a defect density greater than a predetermined defect density; the predetermined defect density is the defect
10 density for which the electrical resistivity of the trapping layer (3) is greater than or equal to 10kohm.cm over a temperature range [-20°C; +120°C].

2. Structure (1,1', 11) for radiofrequency applications according to claim 1, wherein the trapping layer (3) has a
15 resistivity, at 20°C, of greater than 10 kOhm.cm, preferably greater than 50 kOhm.cm.

3. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the difference in thermal expansion coefficient between the trapping layer
20 (3) and the supporting substrate (2) is less than 5 ppm/K between 100°C and 1200°C.

4. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the trapping layer (3) comprises microstructures of a size smaller than
25 20 nm, preferably smaller than 10 nm.

5. Structure (I,I',II) for radiofrequency applications according to any of the above claims, wherein the trapping layer (3) comprises a porous or polycrystalline material.

6. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the trapping layer (3) comprises polycrystalline silicon including 1 to 20% of carbon.

5 7. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the thickness of the trapping layer (3) is between 10 and 50 μm , preferably between 20 and 30 μm .

10 8. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the supporting substrate (2) comprises at least one of the materials selected from the following group: silicon, silicon germanium and silicon carbide.

15 9. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein the resistivity of the supporting substrate (2) is between 10 and 2000 Ohm.cm.

10. Structure (1,1', 11) for radiofrequency applications according to any of the above claims, wherein an active layer (5) is arranged on the trapping layer (3).

20 11. Structure (1,1', 11) for radiofrequency applications according to claim 10, wherein the active layer (5) is formed from a semiconductor material.

25 12. Structure (1,1', 11) for radiofrequency applications according to claim 10, wherein the active layer (5) is formed from a piezoelectric material.

13. Structure (1,1', 11) for radiofrequency applications according to any of claims 10 to 12, wherein the thickness of the active layer (5) is between 10 and 50 μm .

14. Structure (1,1', 11) for radiofrequency applications according to claims 10 to 13, wherein a dielectric layer (4) is arranged between the trapping layer (3) and the active layer (5).

5 15. Structure (1,1', 11) for radiofrequency applications according to claim 14, wherein the dielectric layer (4) is between 10 nm and 6 μm .

16. Structure (1,1', 11) for radiofrequency applications according to any of claims 10 to 15, wherein at least one
10 microelectronic device is present on or in the active layer (5), wherein the microelectronic device is a switching circuit or an antenna adaptation circuit or a radiofrequency power amplification circuit.

17. Structure (1,1', 11) for radiofrequency applications
15 according to any of claims 10 to 16, wherein at least one microelectronic device is present on or in the active layer (5), wherein the microelectronic device comprises a plurality of active components and a plurality of passive components.

18. Structure (1,1', 11) for radiofrequency applications
20 according to any of claims 10 to 16, wherein at least one microelectronic device is present on or in the active layer (5), wherein the microelectronic device comprises at least one control element and one MEMS switching element consisting of an ohmic-contact microswitch or of a capacitive microswitch.

25 19. Structure (1,1', 11) for radiofrequency applications according to claims 10 to 15, wherein at least one microelectronic device is present on or in the active layer (5), wherein the microelectronic device is a radiofrequency filter operating by volume or surface sound wave propagation.