

A DEVICE FOR IMPROVING THE MOBILITY OF CARRIERS IN A
MOSFET CHANNEL ON SILICON CARBIDE

The present invention relates to a device for
5 improving the mobility of carriers in a MOSFET channel on
silicon carbide.

The field of the invention is that of electronic
power components made on silicon carbide (SiC), since
this material presents high carrier saturation speed and
10 very good thermal conductivity. These components include
diodes, thyristors, bipolar transistors, MOSFETs, and
more recently insulated gate bipolar transistors (IGBTs).

The patent US 6 639 273 thus discloses a MOSFET
device on an SiC substrate comprising a channel region 50
15 (p-channel region) having a low concentration of P type
dopant between a source region 43 and a drain region 44,
each of which is of N type (D1, column 5 lines 49 to 61,
Figure 1a). A gate insulating layer 45 is formed
directly on the channel region 50.

20 Nevertheless, it is found that with components of
MOSFET or IGBT type, the mobility of carriers in the
channel is low compared with the mobility that exists in
the core of the material. This gives rise to a limit on
the current-carrying ability of such components. This is
25 due to a high density of interface states between the SiC
and the oxide of the SiO₂ gate. These interface states
are due to the presence of defects such as carbon
clusters or indeed defects in the interface layer under
the oxide that arise at the end of the oxidation process.

30 In this respect, researchers and industry have
developed techniques for improving the quality of the
SiO₂/SiC interface. It is thus known to perform oxidation
under nitrogen oxide NO or N₂O, and on this topic it is
possible to refer to:

35 · G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald,
R.K. Chanana, R.A. Weller, S.T. Pantelides,

L.C. Felldman, O.X. Holland, M.K. Das, and J.W. Palmour -
IEEE Electronic Device Letters **22**, 176 (2001);

· R. Schörner, P. Friedrichs, D. Pstephani,
S. Dimitrijević, and P. Jamet - Applied Physics Letters **80**,
5 4253 (2002);

· L.A. Lipkin, M.K. Das, and J.W. Palmour - Material
Science Forum **389-393**, 985 (2002); and

· K. Shiraishi et al. - First Principle Study of
SiC/SiO₂ Interfaces Towards Future Power Devices -
10 International Electron Device Meeting IEDM 2014
conference proceeding.

Those techniques provide improvements, but they
nevertheless remain insufficient, given the expected
performance.

15 It is also known to perform annealing post-treatment
under nitrogen or by preparing the surface of the SiC
with plasma enhanced chemical vapor deposition (PECVD)
treatment prior to oxidizing the gate. Reference may be
made in particular to Document CN105047539 (A) entitled
20 "Method for improving channel mobility of SiC metal-
oxide-semiconductor-field-effect-transistor (MOSFET)".

Also known is the article "Phosphorous passivation
of the SiO₂/4H-SiC interface" by Y.K. Sharma, A.C. Ahyi,
T. Isaac-Smith, X. Shen, S.T. Pantelides, X. Zhu,
25 L.C. Feldman, and J.R. Williams published in Solid-State
Electronics - volume 68 - February 2012 - pages 103-107.
That involves annealing in an atmosphere filled with P₂O₅
to transform the SiO₂ layer into phosphosilicate glass
(PSG). That also improves the mobility of the carriers.

30 In this example, it is necessary to perform
annealing, with all of the drawbacks that that entails,
and it is difficult to control the quantity of phosphorus
that is introduced. That leads to high levels of
instability while the component is in operation.

35 An object of the present invention is thus to
increase significantly the mobility of carriers in a

MOSFET channel without presenting the above-mentioned limitations of the prior art.

According to the invention, a MOSFET device arranged on a substrate comprises first and second heavily-doped strips respectively covered by first and second contacts, these two strips being spaced apart by a channel that also appears on said substrate, said channel being covered by a dielectric layer, itself surmounted by a third contact; the device is remarkable in that the channel incorporates a lightly-doped thin film at the interface with the dielectric layer, and in that the first and second strips and the thin film present doping of a same type as the channel, in order to create charges that are fixed at the interface between the channel and the dielectric layer so that the carriers are repelled from the dielectric layer and from its defects.

Fixed charges are thus created just at the interface between the channel and the dielectric layer so that the carriers are repelled from the dielectric layer and from its defects.

Advantageously, the substrate is made of silicon carbide.

Preferably, the dielectric layer is made of silicon dioxide.

In a preferred embodiment, the thin film is made by ion implantation.

Thus, by way of example, the ion implantation is performed by plasma-immersion ion implantation.

In a first option, the substrate is of P type and said channel is of N type.

Under such circumstances, the dopant of said thin film is of N type.

For example, the dopant is phosphorus.

In a second option, the substrate is of N type and said channel is of P type.

Under such circumstances, the dopant of said thin film is of P type.

For example, the dopant of the thin film is boron.

Furthermore, the thin film is optionally doped with a dipole-effect element.

For example, the dipole-effect element is fluorine.

5 Preferably, the dipole-effect element is added by plasma-immersion ion implantation.

The present invention can be seen below in greater detail in the context of the following description of embodiments given by way of illustration and with
10 reference to the sole accompanying figure, which is a perspective diagram of a MOSFET device.

With reference to the figure, the device is formed on a substrate 10, which is of type P in the present example. It may be a substrate that is solid, or that is
15 grown epitaxially, or indeed that is grown epitaxially and doped.

On the top face of the substrate 10 there is a first strip 11 (on the left in the figure) that is heavily N⁺ doped. This first strip is commonly called the drain.
20 The drain has a first metal contact 13 applied thereto.

Still on the top face of the substrate 10, there is a second strip 14 (on the right in the figure) that is likewise heavily N⁺ doped. It is arranged parallel to the first strip 11 and at a certain distance therefrom.
25 This second strip 14 is commonly called the source. The source has a second metal contact 15 applied thereto.

The gap that lies between the drain and the source forms a channel 18.

Conventionally, in MOSFET technology, a dielectric
30 layer is added onto the channel between the drain 11 and the source 14. In contrast, according to the invention, a lightly-doped thin film 19 is created on the channel before applying the dielectric layer.

Advantageously, this thin film 19 is made by ion
35 implantation, in particular in plasma immersion mode, which has the advantage of generating fewer defects. It is lightly doped, e.g. with doping being performed at an

acceleration voltage less than 10 kilovolts (kV)
(typically in the range 2 kV to 5 kV), and the implanted
dose is of the order of 10^{14} atoms per square centimeter
(cm^2). The dopant is of type N, and by way of example it
5 may be phosphorus. The plasma is preferably PH_3 or PF_x .
It is also possible to adopt arsenic as the dopant, in
which case the plasma would be of type AsH_3 or AsF_x .

Doping is isotropic and may cover the flanks of a
trench independently of the angle made between the trench
10 and the surface.

It is also desirable for the thin film 19 to have
dipole-effect elements introduced therein, with a first
choice being fluorine. Once more, these elements are
introduced by plasma-immersion ion implantation.

15 A dielectric layer 20 is then deposited on the thin
film 19 in register with the channel 18. In MOSFET
terminology, this layer is commonly referred to as the
gate oxide. It is usually silicon oxide made by thermal
oxidation of the substrate, or by chemical vapor
20 deposition (CVD), or by a combination of both of these
techniques.

It results that the dopant of the thin film 19 is
distributed on both sides of the interface with the
silicon dioxide 20.

25 A third contact 21 is deposited on the gate oxide 20
so as to constitute the gate of the MOSFET device.

Such a configuration provides major advantages
compared with the state of the art.

30 Firstly, the mobility of carriers in the channel
under the gate is multiplied by a factor of more than 3.

Secondly, in the conductive state, the drain/source
current (I_{DS}) is increased by a factor close to 10.

Above, it is assumed that the device is implanted on
a P type substrate.

35 It is entirely possible to apply the invention to a
device implanted on an N type substrate.

Under such circumstances, the drain and the source are heavily doped by means of an element of P+ type.

Similarly, the thin film is then lightly doped with an element of P type, such as boron or aluminum.

5 There is no need to give more details about this second device, since the person skilled in the art can easily transpose the above description for a P type substrate to an N type substrate.

10 In parallel, the doping techniques are identical and any plasmas that are used form part of the state of the art, whether involving boron or indeed aluminum.

 The invention is described with reference to signal-processor MOSFET devices. The invention also applies to vertical power MOSFET devices, or indeed to "trench"
15 transistors.

 The embodiments of the invention described above have been selected for their concrete natures. Nevertheless, it is not possible to list exhaustively all embodiments covered by the invention. In particular, any
20 of the means described may be replaced by equivalent means without going beyond the ambit of the present invention.

CLAIMS

1. A MOSFET device arranged on a substrate (10) comprising first and second heavily-doped strips (11 and 14) respectively covered by first and second contacts (13 and 15), these two strips being spaced apart by a channel (18) that also appears on said substrate (10), said channel being covered by a dielectric layer (20), itself surmounted by a third contact (21); the device being characterized in that said channel (18) incorporates a lightly-doped thin film (19) at the interface with the dielectric layer (20), and in that the first and second strips and the thin film present doping of a same type as the channel, in order to create charges that are fixed at the interface between the channel and the dielectric layer so that the carriers are repelled from the dielectric layer and from its defects.
2. A device according to claim 1, characterized in that said substrate (10) is made of silicon carbide.
3. A device according to either preceding claim, characterized in that said dielectric layer (20) is made of silicon dioxide.
4. A device according to any preceding claim, characterized in that said thin film (19) is made by ion implantation.
5. A device according to the preceding claim, characterized in that the ion implantation is performed by plasma-immersion ion implantation.
6. A device according to any preceding claim, characterized in that said substrate (10) is of P type and said channel (18) is of N type.

7. A device according to the preceding claim,
characterized in that the dopant of said thin film (19)
is of N type.

5 8. A device according to the preceding claim,
characterized in that said dopant is phosphorus.

9. A device according to any one of claims 1 to 5,
characterized in that said substrate (10) is of N type
10 and said channel (18) is of P type.

10. A device according to the preceding claim,
characterized in that the dopant of said thin film (19)
is of P type.

15 11. A device according to the preceding claim,
characterized in that the dopant of said thin film (19)
is boron.

20 12. A device according to any preceding claim,
characterized in that said thin film (19) is doped with a
dipole-effect element.

13. A device according to the preceding claim,
25 characterized in that said dipole-effect element is
fluorine.

14. A device according to claim 11 or claim 12,
characterized in that said dipole-effect element is added
30 by plasma-immersion ion implantation.