Description

This invention relates to a semiconductor device and, more particularly, to an improvement on a contact resistance characteristic between an electrode layer and a semiconductor layer.

With the recent trend for reducing the size and increasing the integration density of integrated circuit elements, great importance has been attached to techniques of forming a conductive layer, e.g., a silicon layer, in contact holes. As a technique for forming a silicon layer in a contact hole, a selective epitaxial growth process has heretofore been used.

Fig. 1 is a sectional view showing a prior art MOS transistor. In the Figure, reference numeral 1 designates a semiconductor substrate of p-conductivity type; numeral 2 is a gate insulation film; numeral 3, a gate electrode; numeral 4, a field oxide film, numeral 5, a non-doped CVD (chemical vapor deposition) SiO_2 (silicon dioxide) film which is formed by CVD process and is not doped with an impurity; numeral 6, a BPSG (boro-phosphosilicate glass) film; numeral 7, a single crystal silicon layer of n-conductivity type; and numerals 8 and 9 are source and drain layers of an n-conductivity type. Numerals 10 and 11 designate respective source and drain electrodes made of aluminum. Silicon layer 7 is formed by the epitaxial growth process. A feature of this structure resides in that BPSG film 6 and n-type silicon layer 7 are not in contact with each other. In the MOS transistor of the above structure, however, the contact resistance between n-type silicon layer 7 and each of aluminum lead layers 10 and 11 on silicon layer 7 fluctuates greatly among individual MOS transistors.

In the above circumstances, it has been desired to reduce fluctuations of the contact resistance between silicon layer 7 and each of aluminum lead layers 10 and 11 with individual elements.

Also, with the above structure the contact resistance between n-type silicon layer 7 and each aluminum lead layer is high, so that non-ohmic contact characteristics result. More specifically, to provide for ohmic contact characteristics of the contact between n-type silicon layer 7 and the aluminum lead layer by reducing the contact resistance therebetween, the impurity concentration of silicon layer 7 has to be set to be 1×10^{20} cm^{-3} or above. In order to increase the impurity concentration of a silicon layer formed in a contact hole by the selective epitaxial growth process, it is necessary to increase the concentration of the doping gas, e.g., PH_3, AsH_3 or B_2H_6. However, increasing the concentration of the doping gas leads to a different problem in that the characteristics of the silicon layer growth are changed. Thus, it has been desired to provide for ohmic contact characteristics of the contact between silicon layer 7 and the aluminum lead layer by reducing the contact resistance therebetween without changing the growth characteristic of silicon layer 7.

Further, while ohmic contact characteristics are obtained between a p-type silicon layer and an aluminum lead layer, the operation speed can be further increased by reducing the contact resistance. For this reason, it has been desired to reduce the contact resistance in the case where a p-type silicon layer is used.

From DE-A-2 825 433 a semiconductor device comprising a semiconductor body of a first conductivity type; an impurity-diffused region of a second conductivity type formed in said semiconductor body; an insulation film formed on said semiconductor film comprising a silicon dioxide film having an impurity of second conductivity type, the insulation film having a contact hole formed on said impurity diffused region; a semiconductor layer of said second conductivity type formed in said contact hole of said insulation film and a conductive layer formed on said semiconductor layer, which also contacts said silicon dioxide film. EP-A-0018175 concerns a semiconductor device according to the pre-characterising portion of claim 1.

An object of the invention is to provide a semiconductor device, in which the contact resistance between a silicon layer and a metal lead layer is low and the contact characteristics is ohmic, to reduce contact resistance fluctuations with individual semiconductor elements, even when the silicon layer is formed in a contact hole using a low concentration doping gas.

According to the present invention, there is provided a semiconductor device comprising: a semiconductor body of a first conductivity type; an impurity diffused region of a second conductivity type formed in said semiconductor body; an insulation structure comprising a first and a second insulation layer, the first insulation layer being formed on said semiconductor body, the second insulation layer being formed on said first insulation layer and containing impurities of said second conductivity type, the first and second insulation layers having a continuous contact hole leading to said impurity diffused region; and a semiconductor layer of said second conductivity type formed on said impurity diffused region and in said continuous contact hole of said first and second insulation layers, **characterized in that** said first and second insulation layers are in contact with said semiconductor layer, said first and second insulation layers are so arranged that the first insulation layer prevents diffusion of impurity from the second insulation layer to the semiconductor substrate; and said semiconductor layer is a single crystal silicon layer

formed by selective epitaxial growth process.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a sectional view showing a prior art semiconductor device;

Fig. 2 is a sectional view showing an embodiment of the semiconductor device according to the invention;

Fig. 3 is a graph showing a contact characteristic between a silicon layer and an Al electrode layer in the embodiment shown in Fig. 2;

Fig. 4 is a sectional view showing another embodiment of the semiconductor device according to the invention; and

Figs. 5 and 6 are sectional views showing further embodiments of the semiconductor device according to the invention.

Now, preferred embodiments of the invention will be described with reference to the drawings. Fig. 2 is a sectional view showing an embodiment of the semiconductor device according to the invention. Parts corresponding to those in the prior art structure of Fig. 1 are designated by the same reference numerals.

N^+-conductivity type impurity diffusion region 8 is formed in a surface region of silicon substrate or well region 1 of a p-conductivity type. SiO_2 (silicon dioxide) film 5, which is not doped with any impurity, is formed on substrate 1 by a CVD (chemical vapor deposition) process. The SiO_2 film is hereinafter referred to as "non-doped CVD SiO_2 film". BPSG (boro-phospho-silicate glass) film 6 is formed on SiO_2 film 5. A contact hole is formed in SiO_2 film 5 and BPSG film 6 to expose impurity diffused region 8. Single crystal silicon layer 7 of an n-conductivity type is formed in the contact hole by the selective epitaxial growth process. Aluminum lead layer 11 is formed on silicon layer 7.

Fig. 3 shows a characteristic relationship curve of a film thickness of silicon layer 7 to the contact resistance formed between silicon layer 7 and aluminum lead layer 11 of a semiconductor device shown in Fig. 2, in which insulating film 6 is a BPSG (boro-phospho-silicate glass) film, SiO_2 film 5 is a non-doped CVD SiO_2 film, single crystal silicon layer 7 is formed by the selective epitaxial growth process and contains 2×10^{19} cm^{-3} of phosphorus, and the contact hole is a 1 μm-square hole. In the Figure, reference character A shows the position of the interface between SiO_2 film 5 and BPSG film 6. As is obvious from this characteristic curve, the contact resistance is too low to present any problem in practice even when the impurity concentration of epitaxially grown silicon layer 7 is set to be as low as 2×10^{19} cm^{-3}.

The reason for the low contact resistance is thought to be that, since silicon layer 7 contacts or is contiguous to BPSG film 6, the n-type impurity of BPSG film 6 is diffused into silicon layer 7 to increase the impurity concentration in the surface region of silicon layer 7. It will be seen from the characteristics of Fig. 3 that BPSG film 6 may be made contiguous to epitaxially grown silicon layer 7 to obtain practically sufficient low contact resistance. The impurity concentration of epitaxially grown silicon layer 7 is desirably 5×10^{18} cm^{-3} or above. If the impurity concentration is below the value noted above, the contact resistance is practically too high even if impurities are diffused from BPSG film 6 into silicon layer 7.

In the Fig. 2 embodiment, n^+-type impurity diffused region 8 is used. However, a p-type impurity diffused region can be used. In this case, the silicon substrate or well region is of n-conductivity type, and the epitaxially grown silicon layer is of p-conductivity type. Also, in this case, BSG (boro-silicate glass) or BAs SG (boro-arseno silicate glass) may be used as insulation film 6. The impurity concentration of the epitaxially grown p-type silicon layer is desirably 5×10^{18} cm^{-3} or above.

Fig. 4 is a sectional view showing another embodiment of the semiconductor device according to the invention. This device corresponds to the prior art device shown in Fig. 1.

Field oxide film 4 of a predetermined pattern is formed on silicon substrate or well region 1 of a p-conductivity type. Impurity-diffused regions 8 and 9 of an n^+-conductivity type are formed in the element forming regions of silicon substrate 1, which are defined by the predetermined pattern of field oxide film 4. Impurity-diffused regions 8 and 9 form source and drain regions, respectively. SiO_2 film 5 is formed on field oxide film 4 and gate insulation film 2. SiO_2 film 5 is formed by CVD (chemical vapor deposition) process and undoped with any impurities. BPSG film 6 is formed on SiO_2 film 5. Contact holes are formed in SiO_2 film 5 and BPSG film 6. The contact holes lead to source region 8 and drain region 9. Single crystal silicon layers 7 are formed in the contact holes leading to source region 8 and drain region 9. Single crystal silicon layers 7 are formed by a selective epitaxial growth process. Source electrode 10 made of aluminum is formed on silicon layer 7 on source region 8. Drain electrode 11 made of aluminum is formed on silicon layer 7 on drain region 9. Silicon layers 7 contact or are contiguous to BPSG film 6. A further hole is formed in SiO_2 film 4 and BPSG film 6, which leads to gate insulation film 2. Gate electrode 3 made of aluminum is formed in the hole.

A feature of this embodiment, like the embodiment of Fig. 2, resides in that silicon layer 7 and BPSG film 6 are contiguous to each other. SiO_2

film 5 has an effect of preventing the diffusion of boron (B) and phosphorus (P) in BPSG film 6 into semiconductor substrate 1.

In the Fig. 4 embodiment, n^+-type impurity diffused regions 8 and 9 are used. However, p-type impurity diffused regions can be used. In this case, the silicon substrate or well region is of n-conductivity type, and the epitaxially grown silicon layers are of p-conductivity type.

Now, examples of the invention will be given.

Example 1

A 256K SRAM (static random access memory) having an n-channel MOS transistor structure shown in Fig. 4 was trial manufactured under the 1.2 μm design rule (a minimum contact hole size). N-type silicon layers with a thickness of 1 μm and a phosphorus concentration of 4×10^{19} cm^{-3} were formed, using a reactive gas of H_2, SiH_2Cl_2, HCl and PH_3, in contact holes for exposing the source and drain regions of the n-channel MOS transistor, by a selective epitaxial growth process. Then, an aluminum lead layer was formed on the n-type silicon layers on the source and drain regions. Interlayer insulation films 5 and 6 were constituted by non-doped CVD SiO_2 film 5 and BPSG film 6. The thickness of BPSG film 6 and SiO_2 films 5 was set to 0.5 μm.

Example 2

The same SRAM as Example 1 was trial manufactured except that the phosphorus concentration of silicon layer 7 was set to 3×10^{18} cm^{-3}.

Example 3

The same SRAM as Example 1 was trial manufactured except that AsH_3 was used as the doping gas and that the As concentration in silicon layer 7 was set to 4×10^{19} cm^{-3}.

Example 4

The same SRAM as Example 1 was trial manufactured except that interlayer insulation films 5 and 6 were non-doped CVD SiO_2 film 5 and PSG film 6 and the thickness of SiO_2 film 5 and PSG film 6 was set to 0.5 μm.

Example 5

The same SRAM as Example 1 was trial manufactured except that the MOS transistor was a p-type MOS transistor, a reactive gas composed of H_2, SiH_2Cl_2, HCl and B_2H_6 was used, the silicon layer was a p-type silicon layer formed by the selective epitaxial growth process and having a thickness of 1 μm and a boron concentration of 4×10^{19} cm^{-3}, interlayer insulation films 5 and 6 were non-doped CVD SiO_2 film 5 and BSG film 6, and the thickness of CVD SiO_2 film 5 and BSG films 6 was set to 0.5 μm.

Contrast Example 1

The same SRAM as Example 1 was trial manufactured except that the thickness of silicon layer 7 was set to 0.4 μm.

Contrast Example 2

The same SRAM as Example 1 was trial manufactured except that interlayer insulation films 5 and 6 were non-doped CVD SiO_2 film 5 and BSG film 6, and the thickness of CVD SiO_2 film 5 and BSG film 6 was set to 0.5 μm.

Contrast Example 3

The same SRAM as Example 5 was trial manufactured except that the thickness of the silicon layer was set to 0.4 μm.

The operating characteristics of the individual examples of 256K SRAMs were compared to those of the contrast examples. In Examples 1 to 5, all 256K SRAMs were operated. In Contrast Examples 1 and 3, some 256K SRAMs were operational, but others were not. In Contrast Example 2, no 256K SRAMs were operational.

In contrast Examples 1 and 3 of 256K SRAMs, the contact resistance between the silicon layer and aluminum lead layer fluctuated greatly among the individual MOS transistors. In contrast Example 2 of 256K SRAMs, the contact resistance was high in all the MOS transistors.

The reason for the fluctuations of the contact resistance among the individual MOS transistors in constrast Examples 1 and 3 of 256K SRAMs is thought to be due to the lack of uniformity of the film thickness of silicon layer 7 of the individual MOS transistors. More specifically, in contrast Example 1 of 256K SRAMs, the contact resistance is low in the MOS transistors where silicon layer 7 is contiguous to BPSG film 6, while it is high in the MOS transistors where silicon layer 7 is not contiguous to BPSG film 6.

In contrast Example 1 of the SRAM, the MOS transistors where silicon layer 7 are contiguous to BPSG film 6 are operative owing to low contact resistance, but the MOS transistors where the two layers are not contiguous are not operative because of high contact resistance. The same thing can be said of contrast Example 3 of the SRAM. That is, the MOS transistors where silicon layer 7 is

contiguous to BSG film 6 are operative owing to low contact resistance, but the MOS transistors where the two layers are not contiguous are not operative because of high contact resistance.

The reason that all the SRAMs in contrast Example 2 fail to operate is thought to be due to high contact resistance, since silicon layer 7 is not contiguous to BPSG film 6 in all the MOS transistors.

In Examples 1 to 5, all SRAMs were normally operational. More specifically, with each SRAM MOS transistor the contact resistance was low, and contact resistance fluctuations were low among the individual MOS transistors.

In Example 2 of the SRAM, the contact resistance of each MOS transistor is approximately three times that of each SRAM transistor in Examples 1, 3 and 4, so that the operation speed is lower than that of Examples 1, 3 and 4.

It is seen from Example 2 that more superior operation characteristics can be obtained by setting the impurity concentration of the silicon layer to be 4×10^{18} cm^{-3} or above. Further, it will be seen that the invention is applicable not only to the n-type contact but also to the p-type contact as shown in Example 5.

Fig. 5 is a sectional view showing a further embodiment of the semiconductor device of the invention. In this embodiment, molybdenum (Mo) layer 13 is formed between single crystal silicon layer 7 and aluminum lead layer 11. Molybdenum has a low work-function, and the contact resistance between silicon layer 7 and aluminum lead layer 11 is small. Thus, the ohmic resistance characteristic is improved. Titanium, tungsten or tantalum may be used instead of molybdenum. An alloy of titanium and tungsten may also used. Molybdenum silicide, tungsten silicide, titanium silicide, or tantalum silicide may be used. Titanium nitride may also be used. These materials have low work-functions, and the contact resistance between silicon layer 7 and aluminum lead layer 11 is made low. Thus, the ohmic resistance characteristic is improved.

Fig. 6 is a sectional view showing a still further embodiment of the semiconductor device of the invention. Also in this embodiment, molybdenum layers 13 are formed between single crystal silicon layer 7 and each of aluminum lead layers 10 and 11. Also in this embodiment, the materials mentioned above may be used in place of molybdenum. These materials have low work-functions, and the contact resistance between silicon layer 7 and each of aluminum lead layers 10 and 11 is made low. Thus, the ohmic resistance characteristic is improved.

When silicon layer 7 is n-type, silicon oxide layer 6 is not limited to BPSG or PSG, but it is possible to use AsSG, BAsSG, PAsSG and BPAsSG. Further, where the silicon layer is of a p-type, either BSG or BAsSG may be used as silicon oxide layer 6.

As has been described in the foregoing, according to the invention, it is possible to provide a semiconductor device in which the contact resistance of the contact between a semiconductor layer formed in a contact hole and a metal lead layer formed on the semiconductor layer and also fluctuations of the contact resistance are low so that improved operation characteristics can be obtained.

Claims

1. A semiconductor device comprising:

a semiconductor body (1) of a first conductivity type;

an impurity diffused region (8,9) of a second conductivity type formed in said semiconductor body (1);

an insulation structure comprising a first and a second insulation layer (5,6), the first insulation layer (5) being formed on said semiconductor body, the second insulation layer (6) being formed on said first insulation layer and containing impurities of said second conductivity type, the first and second insulation layers having a continuous contact hole leading to said impurity diffused region; and

a semiconductor layer (7) of said second conductivity type formed on said impurity diffused region and in said continuous contact hole of said first and second insulation layers, and a conductive layer (10,11) formed on said semiconductor layer,

said first and second insulation layers (5,6) are in contact with said semiconductor layer (7),

said first and second insulation layers (5,6) are so arranged that the first insulation layer (5) prevents diffusion of impurity from the second insulation layer to the semiconductor substrate; **characterized in that**

said semiconductor layer is a single crystal silicon layer formed by selective epitaxial growth process.

2. A semiconductor device according to claim 1, **characterized in that**

said semiconductor body (1) is a silicon substrate, said silicon dioxide film (6) is a film formed of one component selected from the group consisting of phospho-silicate glass, arseno-silicate glass, boro-phospho-silicate glass, boro-arseno-silicate glass, phospho-arseno-silicate glass, and boro-phospho-arseno-silicate glass, said first conductivity type and second conductivity type are p-con-

contiguous to BSG film 6 are operative owing to low contact resistance, but the MOS transistors where the two layers are not contiguous are not operative because of high contact resistance.

The reason that all the SRAMs in contrast Example 2 fail to operate is thought to be due to high contact resistance, since silicon layer 7 is not contiguous to BPSG film 6 in all the MOS transistors.

In Examples 1 to 5, all SRAMs were normally operational. More specifically, with each SRAM MOS transistor the contact resistance was low, and contact resistance fluctuations were low among the individual MOS transistors.

In Example 2 of the SRAM, the contact resistance of each MOS transistor is approximately three times that of each SRAM transistor in Examples 1, 3 and 4, so that the operation speed is lower than that of Examples 1, 3 and 4.

It is seen from Example 2 that more superior operation characteristics can be obtained by setting the impurity concentration of the silicon layer to be 4×10^{18} cm^{-3} or above. Further, it will be seen that the invention is applicable not only to the n-type contact but also to the p-type contact as shown in Example 5.

Fig. 5 is a sectional view showing a further embodiment of the semiconductor device of the invention. In this embodiment, molybdenum (Mo) layer 13 is formed between single crystal silicon layer 7 and aluminum lead layer 11. Molybdenum has a low work-function, and the contact resistance between silicon layer 7 and aluminum lead layer 11 is small. Thus, the ohmic resistance characteristic is improved. Titanium, tungsten or tantalum may be used instead of molybdenum. An alloy of titanium and tungsten may also used. Molybdenum silicide, tungsten silicide, titanium silicide, or tantalum silicide may be used. Titanium nitride may also be used. These materials have low work-functions, and the contact resistance between silicon layer 7 and aluminum lead layer 11 is made low. Thus, the ohmic resistance characteristic is improved.

Fig. 6 is a sectional view showing a still further embodiment of the semiconductor device of the invention. Also in this embodiment, molybdenum layers 13 are formed between single crystal silicon layer 7 and each of aluminum lead layers 10 and 11. Also in this embodiment, the materials mentioned above may be used in place of molybdenum. These materials have low work-functions, and the contact resistance between silicon layer 7 and each of aluminum lead layers 10 and 11 is made low. Thus, the ohmic resistance characteristic is improved.

When silicon layer 7 is n-type, silicon oxide layer 6 is not limited to BPSG or PSG, but it is possible to use AsSG, BAsSG, PAsSG and BPAsSG. Further, where the silicon layer is of a p-type, either BSG or BAsSG may be used as silicon oxide layer 6.

As has been described in the foregoing, according to the invention, it is possible to provide a semiconductor device in which the contact resistance of the contact between a semiconductor layer formed in a contact hole and a metal lead layer formed on the semiconductor layer and also fluctuations of the contact resistance are low so that improved operation characteristics can be obtained.

Claims

1. A semiconductor device comprising:
   a semiconductor body (1) of a first conductivity type;
   an impurity diffused region (8,9) of a second conductivity type formed in said semiconductor body (1);
   an insulation structure comprising a first and a second insulation layer (5,6), the first insulation layer (5) being formed on said semiconductor body, the second insulation layer (6) being formed on said first insulation layer and containing impurities of said second conductivity type, the first and second insulation layers having a continuous contact hole leading to said impurity diffused region; and
   a semiconductor layer (7) of said second conductivity type formed on said impurity diffused region and in said continuous contact hole of said first and second insulation layers, and a conductive layer (10,11) formed on said semiconductor layer,
   said first and second insulation layers (5,6) are in contact with said semiconductor layer (7),
   said first and second insulation layers (5,6) are so arranged that the first insulation layer (5) prevents diffusion of impurity from the second insulation layer to the semiconductor substrate; **characterized in that**
   said semiconductor layer is a single crystal silicon layer formed by selective epitaxial growth process.

2. A semiconductor device according to claim 1, **characterized in that**
   said semiconductor body (1) is a silicon substrate, said silicon dioxide film (6) is a film formed of one component selected from the group consisting of phospho-silicate glass, arseno-silicate glass, boro-phospho-silicate glass, boro-arseno-silicate glass, phospho-arseno-silicate glass, and boro-phospho-arseno-silicate glass, said first conductivity type and second conductivity type are p-con-

ductivity type and n-conductivity type, respectively, and said single crystal silicon layer (7) is of n-conductivity type.

4. A semiconductor device according to claim 1, **characterized in that** said semiconductor body (1) is a silicon substrate, said silicon dioxide film (6) is a film formed of one component selected from the group consisting of boro-silicate glass and boro-arseno-silicate glass, said first conductivity type and second conductivity type are n-conductivity type and p-conductivity type, respectively and said single crystal silicon layer (7) is of p-conductivity type.

Patentansprüche

1. Eine Halbleitervorrichtung umfassend:
einen Halbleiterkörper (1) eines ersten Leitfähigkeitstyps;
einen in besagtem Halbleiterkörper (1) gebildeten, eindiffundierte Fremdatome aufweisenden Bereich (8,9) eines zweiten Leitfähigkeitstyps;
eine eine erste und eine zweite Isolierschicht (5,6) umfassende Isolierstruktur, wobei die erste Isolierschicht (5) auf besagtem Halbleiterkörper gebildet ist, wobei die zweite Isolierschicht (6) auf besagter erster Isolierschicht gebildet ist und Fremdatome des besagten zweiten Leitfähigkeitstyps enthält, und wobei die erste und zweite Isolierschicht ein durchgehendes, zu besagtem Bereich mit eindiffundierten Fremdatomen führendes Kontaktfenster besitzen; und
eine auf besagtem Bereich mit eindiffundierten Fremdatomen und in besagtem durchgehendem Kontaktfenster der besagten ersten und zweiten Isolierschicht gebildete Halbleiterschicht (7) des besagten zweiten Leitfähigkeitstyps, und eine auf besagter Halbleiterschicht gebildete leitende Schicht (10,11),
wobei besagte erste und zweite Isolierschicht (5,6) in Kontakt mit besagter Halbleiterschicht (7) stehen,
wobei besagte erste und zweite Isolierschicht (5,6) so angeordnet sind, daß die erste Isolierschicht (5) die Diffusion von Fremdatomen aus der zweiten Isolierschicht (6) zum Halbleitersubstrat verhindert; dadurch gekennzeichnet,
daß besagte Halbleiterschicht eine durch ein selektives Epitaxie-Verfahren gebildete einkristalline Siliziumschicht ist.

2. Eine Halbleitervorrichtung nach Anspruch 1, dadurch gekennzeichnet,
daß besagter Halbleiterkörper (1) ein Siliziumsubstrat ist, daß besagter Siliziumdioxidfilm (6) ein Film ist, der aus einem Bestandteil gebildet ist, welcher aus der aus Phosphorsilikatglas, Arsensilikatglas, Borphosphorsilikatglas, Borarsensilikatglas, Phosphorarsensilikatglas und Borphosphorarsensilikatglas bestehenden Gruppe ausgewählt ist, daß besagter erste Leitfähigkeitstyp und zweiter Leitfähigkeitstyp ein p-Leitfähigkeitstyp bzw. ein n-Leitfähigkeitstyp sind, und daß besagte einkristalline Siliziumschicht (7) vom n-Leitfähigkeitstyp ist.

3. Eine Halbleitervorrichtung nach Anspruch 1, dadurch gekennzeichnet,
daß besagter Halbleiterkörper (1) ein Siliziumsubstrat ist, daß besagter Siliziumdioxidfilm (6) ein Film ist, der aus einem Bestandteil gebildet ist, welcher aus der aus Borsilikatglas und Borarsensilikatglas bestehenden Gruppe ausgewählt ist, daß besagter erster Leitfähigkeitstyp und zweiter Leitfähigkeitstyp ein n-Leitfähigkeitstyp bzw. ein p-Leitfähigkeitstyp sind, und daß besagte einkristalline Siliziumschicht (7) vom p-Leitfähigkeitstyp ist.

Revendications

1. Dispositif à semiconducteur, comprenant :
un corps semiconducteur (1) d'un premier type de conductivité;
une région (8, 9) ayant subi une diffusion d'impuretés, d'un deuxième type de conductivité, formée dans ledit corps semiconducteur (1);
une structure d'isolation comprenant une première et une deuxième couche d'isolation (5, 6), la première couche d'isolation (5) étant formée sur ledit corps semiconducteur, la deuxième couche d'isolation (6) étant formée sur ladite première couche d'isolation et contenant des impuretés dudit deuxième type de conductivité, les première et deuxième couches d'isolation ayant un trou de contact continu qui conduit à ladite région ayant subi une diffusion d'impuretés;
une couche semiconductrice (7) dudit deuxième type de conductivité, formée sur ladite région ayant subi une diffusion d'impuretés et dans ledit trou de contact continu desdites première et deuxième couches d'isolation ; et
une couche conductrice (10, 11) formée sur ladite couche semiconductrice ;
lesdites première et deuxième couches d'isolation (5, 6) étant en contact avec ladite couche semiconductrice (7),

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lesdites première et deuxième couches d'isolation (5, 6) étant ainsi disposées que la première couche d'isolation (5) empêche la diffusion d'impuretés de la deuxième couche d'isolation au substrat semiconducteur ;

caractérisé en ce que ladite couche semiconductrice est une couche de silicium monocristallin formée par un processus de croissance épitaxiale sélective.

2. Dispositif à semiconducteur selon la revendication 1, caractérisé en ce que ledit corps semiconducteur (1) est un substrat de silicium, ladite pellicule de dioxyde de silicium (6) est une pellicule formée d'un composant choisi dans le groupe comprenant le verte de phosphosilicate, le verte d'arséniosilicate, le verte de borophosphosilicate, le verte de boroarséniosilicate, le verte de phosphoarséniosilicate et le verte de borophosphoarséniosilicate, lesdits premier type de conductivité et deuxième type de conductivité sont respectivement le type p de conductivité et le type n de conductivité, et ladite couche de silicium monocristallin (7) est du type de conductivité n.

3. Dispositif à semiconducteur selon la revendication 1, caractérisé en ce que ledit corps semiconducteur (1) est un substrat de silicium, ladite pellicule de dioxyde de silicium (6) est une pellicule formée d'un composant choisi dans le groupe comprenant le verte de borosilicate et le verte de boroarséniosilicate, lesdits premier type de conductivité et deuxième type de conductivité sont respectivement le type n de conductivité et le type p de conductivité, et ladite couche de silicium monocristallin (7) est du type de conductivité p.