WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

first semiconductor patterns vertically stacked on a substrate and vertically spaced apart from each other;

second semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other; and

a first gate electrode on the first semiconductor patterns; and

a second gate electrode on the second semiconductor patterns;

the first gate electrode comprising:

a first work function metal pattern on a top surface, a bottom surface, and sidewalls of respective ones of the first semiconductor patterns;

a barrier pattern on the first work function metal pattern; and

a first electrode pattern on the barrier pattern; and

the second gate electrode comprising:

a second work function metal pattern on a top surface, a bottom surface, and sidewalls of respective ones of the second semiconductor patterns; and

a second electrode pattern on the second work function metal pattern;

wherein the first gate electrode has a first part between adjacent ones of the first semiconductor patterns,

wherein the barrier pattern and the first electrode pattern are spaced apart from the first part,

wherein the barrier pattern comprises a first metal nitride layer comprising silicon,

wherein the second work function metal pattern comprises a second metal nitride layer comprising silicon,

wherein the second work function metal pattern comprises a work function less than that of the first work function metal pattern; and

wherein the second work function metal pattern comprises a silicon concentration that varies based on a distance from the substrate.

2. The semiconductor device of claim 1, wherein the first gate electrode has a second part on an uppermost one of the first semiconductor patterns,

wherein the first part comprises the first work function metal pattern, and

wherein the second part comprises the first work function metal pattern, the barrier pattern, and the first electrode pattern that are sequentially stacked.

3. The semiconductor device of claim 1, wherein the first work function metal pattern comprises a third metal nitride layer.

4. The semiconductor device of claim 1,

wherein the barrier pattern comprises a silicon concentration greater than that of the second work function metal pattern.

5. The semiconductor device of claim 1, wherein the second work function metal pattern comprises work function metal layers and an intermediate layer between the work function metal layers,

wherein respective ones of the work function metal layers comprise the second metal nitride layer comprising silicon, and

wherein the intermediate layer comprises a silicon layer.

6. The semiconductor device of claim 1, wherein the second gate electrode has a first part between adjacent ones of the second semiconductor patterns and a second part on an uppermost one of the second semiconductor patterns,

wherein the first part of the second gate electrode comprises the second work function metal pattern, and

wherein the second part of the second gate electrode comprises the second work function metal pattern and the second electrode pattern that are sequentially stacked.

7. The semiconductor device of claim 1, further comprising:

third semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other; and

a third gate electrode on the third semiconductor patterns, the third gate electrode comprising:

a third work function metal pattern on a top surface, a bottom surface, and sidewalls of respective ones of the third semiconductor patterns; and

a third electrode pattern on the third work function metal pattern,

wherein the first work function metal pattern comprises a first work function metal layer,

wherein the third work function metal pattern comprises the first work function metal layer and a second work function metal layer, and

wherein the second work function metal layer comprises a work function less than that of the first work function metal layer.

8. The semiconductor device of claim 1, wherein the barrier pattern comprises a silicon concentration ranging from 20 at% to 50 at%.

9. The semiconductor device of claim 1, wherein the first electrode pattern comprises a resistance less than that of the first work function metal pattern, and

wherein the first electrode pattern comprises aluminum, tungsten, titanium, and/or tantalum.

10. A semiconductor device, comprising a first transistor and a second transistor on a substrate, each of the first and second transistors comprising:

semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other; and

a gate electrode on the semiconductor patterns,

wherein the gate electrode of the first transistor comprises a first work function metal pattern and a first electrode pattern that are sequentially stacked on an uppermost one of the semiconductor patterns of the first transistor,

wherein the gate electrode of the second transistor comprises a second work function metal pattern, a barrier pattern, and a second electrode pattern that are sequentially stacked on an uppermost one of the semiconductor patterns of the second transistor,

wherein the first electrode pattern covers the first work function metal pattern,

wherein the first work function metal pattern comprises a silicon-containing first metal nitride layer, and

wherein the first work function metal pattern comprises a silicon concentration that varies based on a distance from the substrate.

11. The semiconductor device of claim 10, wherein the barrier pattern comprises a silicon-containing metal nitride layer.

12. The semiconductor device of claim 10,

wherein the second work function metal pattern comprises a second metal nitride layer.

13. The semiconductor device of claim 10, wherein the first and second electrode patterns comprise aluminum, tungsten, titanium, and/or tantalum.

14. The semiconductor device of claim 10, wherein the gate electrode of the first transistor and the gate electrode of the second transistor each comprise a first part between adjacent ones of the semiconductor patterns,

wherein the first electrode pattern is spaced apart from the first part of the gate electrode of the first transistor, and

wherein the second electrode pattern and the barrier pattern are spaced apart from the first part of the gate electrode of the second transistor.

15. A semiconductor device, comprising:

first semiconductor patterns vertically stacked on a substrate;

second semiconductor patterns vertically stacked on the substrate;

a first gate electrode on the first semiconductor patterns; and

a second gate electrode on the second semiconductor patterns,

wherein the first gate electrode comprises:

a first work function metal pattern within a space between adjacent ones of the first semiconductor patterns and on a top surface, a bottom surface, and sidewalls of respective ones of the first semiconductor patterns; and

a first electrode pattern on the first work function metal pattern, and

wherein the second gate electrode comprises:

a second work function metal pattern within a space between adjacent ones of the second semiconductor patterns and on a top surface, a bottom surface, and sidewalls of respective ones of the second semiconductor patterns;

a second electrode pattern on the second work function metal pattern; and

a barrier pattern between the second work function metal pattern and the second electrode pattern,

wherein the first work function metal pattern comprises a silicon-containing first metal nitride layer,

wherein the second work function metal pattern comprises a second metal nitride layer,

wherein the barrier pattern comprises a silicon-containing third metal nitride layer, and

wherein the barrier pattern comprises a silicon concentration greater than that of the first work function metal pattern; and

wherein the first work function metal pattern comprises a silicon concentration that varies based on a distance from the substrate.

16. The semiconductor device of claim 15, wherein the first electrode pattern is spaced apart from the space between adjacent ones of the first semiconductor patterns by at least one of the first semiconductor patterns in a vertical direction, and

the second electrode pattern and the barrier pattern are spaced apart from the space between adjacent ones of the second semiconductor patterns by at least one of the second semiconductor patterns.

17. The semiconductor device of claim 15, wherein the first semiconductor patterns and the first gate electrode are portions of a first transistor,

wherein the second semiconductor patterns and the second gate electrode are portions of a second transistor,

wherein the first and second transistors are PMOSFETs, and

wherein the first transistor has a threshold voltage greater than that of the second transistor.

18. The semiconductor device of claim 15, wherein the silicon concentration of the barrier pattern falls within a range from 20 at% to 50 at%.