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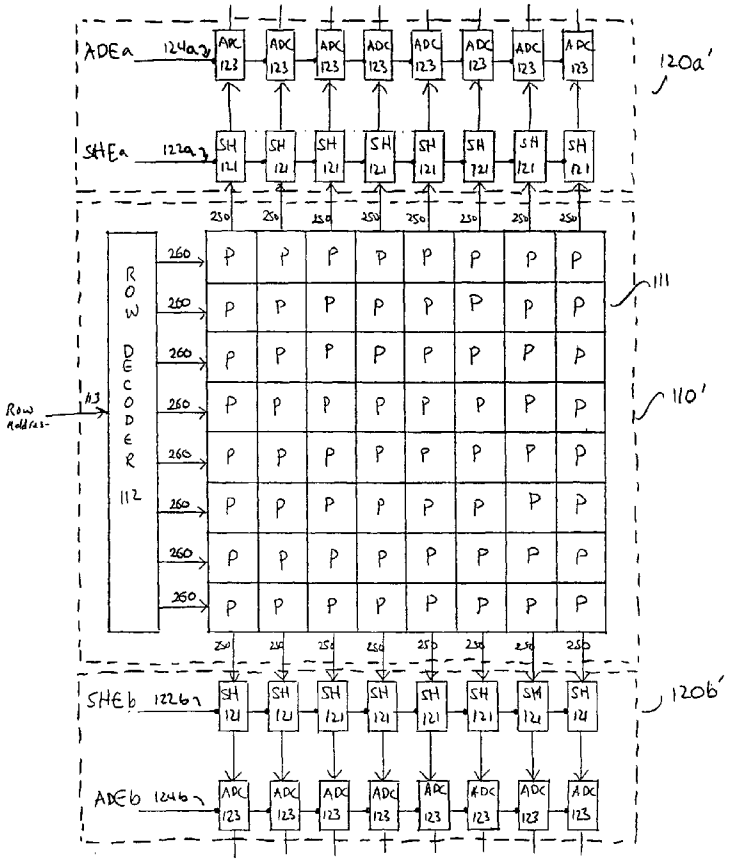
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(54) Title: DOUBLING OF SPEED IN CMOS SENSOR WITH COLUMN-PARALLEL ADCS



(57) Abstract: An imaging system features high speed digitization of pixel signals by utilizing top and bottom digitization circuits which pipeline sample-and-hold operations with analog-to-digital conversion. In operation, while one digitization circuit is performing a sample-and-hold operation, the other digitization circuit is performing analog-to-digital conversion. The speed of the imaging system may be further increased by pipelining and interleaving operations within the top and bottom digitization circuits by using additional sets of sample-and-hold circuits and analog-to-digital converters.

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