

Method for Dynamic Range Reduction in a Wideband Receiver

FIELD OF THE INVENTION

The present invention relates generally to wideband receivers, and, more specifically, to an adaptive technique for suppressing unwanted signals to reduce the dynamic-range requirement of a digitizer in a wideband receiver.

BACKGROUND

Analog-to-digital conversion remains as the main bottleneck in realising a wideband software radio receiver 100, such as the one illustrated in Fig. 1. The receiver 100 receives signals via an antenna 110. The receiver 100 consists of a wideband radiofrequency (RF) front-end 120, a digitizer or analog-to-digital conversion (ADC) device 130, and a channelization filter 140. The wideband RF front-end 120 processes the received signal from antenna 110. The output of the front-end 120 is digitized by the ADC 130. The digitized output of ADC 130 is filtered by the channelization filter 140 to provide a digital signal to a signal processing block (not shown). An example of a relevant wideband receiver is the software-radio receiver described by Kenington, P.B., "Emerging technologies for software radio", *Electronics & Communication Engineering Journal*, April 1999, pp. 69-83.

The stringent dynamic-range requirements for the ADC 130 arises from the fact that the channelization function 140 of the wide-band receiver 100 is carried out digitally. The ADC 130 is hence exposed to wideband radio signals, which may contain strong interfering signals. Such requirements cannot be fulfilled by existing systems. The stringent requirements for ADC dynamic range inhibit the implementation of a wideband receiver. The techniques for solving this problem are related to research areas such as dynamic range reduction in multi-carrier signal processing and interference cancellation. Some of the existing techniques which attempt to address the ADC dynamic range problem for a wideband receiver, are summarized below.

U.S. Patent No. 6,195,537 issued to Allpress et al on February 27, 200 and entitled "Method and apparatus for strong signal suppression in multi-carrier signals" relates to the digitisation of multi-carrier signals. The described system comprises a strong signal suppressor that selectively suppresses stronger signals at certain carriers without affecting weaker signals. The stronger signals have to go through a lengthy sequence of operations. Those signals are firstly coarsely digitized, then are detected by scanning, are scaled, undergo phase correction, subsequently are converted back to the analog domain where a reconstruction operation is carried out, and finally are recombined with the received signal in such a way that the stronger signals are attenuated.

One significant disadvantage of the system of U.S. Patent No. 6,195,537 is its complexity. Suppression of strong signals requires a lengthy sequence of operations, e.g. scanning and phase correction that are relatively complicated. Moreover, the system does not distinguish between the interference and desired signal, which may lead to distortion of the desired signal by the suppression process if the desired signal is strong. More specifically, being stronger than interfering signals, the desired signal is selected by scanning to be essentially scaled and phase-corrected to suppress the original desired signal. These operations unnecessarily attenuate, and inevitably distort, the desired signal.

U.S. Patent No. 5,826,181 issued to Reed on October 20, 1998 and entitled "Radio frequency noise reduction arrangement" describes a strong interfering signal in the received signal being reconstructed and tracked using a Phase Lock Loop (PLL). Interference suppression is achieved by combining the phase-inverted and scaled PLL output with the original received signal. Since the system of US Patent No. 5,826,181 involves a PLL, the system can only track a narrow-band signal modulated at a single carrier frequency, which is always the signal with the largest power. This scheme does not work if the desired signal is stronger than, or has the same power as, the blocking signals, because the desired signal is locked by the PLL and hence suppressed. Another disadvantage arises when multiple strong blocking signals are present. The PLL may fail to track any of the blocking signals, or the suppression of one of the blocking signals may not be sufficient in reducing the dynamic range of the received signal.

U.S. Patent No. 5,694,395 issued to Myer et al on December 2, 1997 and entitled "Method and apparatus for processing multicarrier signals" describes the design of a multi-carrier signal processor. The received signals at different carriers are separated, modified using individual sets of processors, and combined with a delayed version of the received signal. The modification of the signals ensures that the combined signal has a reduced dynamic range.

U.S. Patent No. 3,938,153 issued to Lewis et al on February 10, 1976 and entitled "Sidelobe canceller system" describes isolating interfering blocking signals using several filters with different bandwidths and/or downconversion with multiple local oscillators (LO) and subtracting from the noise mixed downconverted signal.

The main drawback of the schemes in U.S. Patent No. 5,694,395 and U.S. Patent No. 3,938,153 is the system complexity. By integrating a number of antennas, local oscillators (Los), mixers, bandpass filters, and subtractors, the receiver complexity and power consumption is significantly increased while the flexibility of the system is greatly reduced due to the extensive employment of analog components.

A need therefore exists for an all rounded solution to provide high dynamic-range for a wideband receiver and alleviate the ADC requirements.

SUMMARY

In accordance with a first aspect of the invention, a method for processing an input wideband signal containing a desired signal and a plurality of interfering signals is disclosed. The input wideband signal is split into a first signal for a first signal path and a second signal for a second signal path. The first and second signals are each an analog representation of the input wideband signal. The second signal is digitized to provide a digitized second signal. The desired signal is suppressed in the digitized second signal to provide a plurality of interference-dominant signals. A phase shift is applied to the plurality of interference-dominant signals to provide a plurality of digital, phase-shifted signals through the second path that is substantially the same as a phase shift through the first path. The plurality of digital, phase-shifted signals are converted into analog form to

provide a plurality of analog regenerated signals. The plurality of analog regenerated signals from the second signal path and the first signal from the first signal path are combined to provide an interference-suppressed, input wideband signal based on a difference of the plurality of analog regenerated signals and the first signal.

The interference-suppressed, wideband input signal may also be digitized to provide a digitised interference-suppressed input signal. Further, the desired signal may be extracted from the digitised interference-suppressed input signal. The suppressing step may be implemented using a digital filter and the extracting step may be implemented using a channelization filter. Further, coefficients of the digital filter and the digital channelization filter may be changed to extract a different desired signal from the digitised interference-suppressed input signal.

The phase-shift applying step may be implemented using a phase-shifting circuit. The digitised interference-suppressed input signal may be received and coefficients of the phase shifting circuit may be changed.

The digitised interference-suppressed input signal and the plurality of digital, phase-shifted signals may be combined to provide a digitised wideband input signal.

Optionally, a delay through the first path may be made equal to a delay through the second signal path. The amplitude of the second signal may also be controlled. The second signal may further be scaled to provide a scaled second signal that swings over approximately the maximum input range of the digitizing means. The amplitude of the interference-suppressed, input wideband signal may be controlled. The interference-suppressed, input wideband signal may be scaled to provide a scaled interference-suppressed, input wideband signals that swings over approximately the maximum input range of the digitizing means.

The phase-shifting applying step may be implemented using an adaptive filter having coefficients that can be constantly updated using a filter-weight-updating algorithm so that variation of the characteristics of the input wideband signal is able to be tracked.

In accordance with a second aspect of the invention, a method for processing an input wideband signal containing a desired signal and a plurality of interfering signals is disclosed. An analog interference cancellation signal is subtracted from an input wideband signal to provide an interference-suppressed signal. The interference-suppressed signal is digitized to provide a digitized signal. The desired signal in the digitized signal is suppressed to provide a reference interference signal. The reference interference signal is filtered based on filter parameters from the digitised signal to provide a digital interference cancellation signal. The digital interference cancellation signal is converted into analog form to provide the analog interference cancellation signal.

The digital interference cancellation signal and the digitized signal after cancellation may be combined to provide a reconstructed digitized signal for input to the suppressing step. Further, a delay in a signal path for the interference-suppressed signal may be made equal to a delay through a signal path for the reference interference signal from the suppressing step. The desired signal may be extracted from the digitised interference-suppressed signal.

The suppressing step may be implemented using a digital filter and the extracting step may be implemented using a digital channelization filter. Further, coefficients of the digital filter and the digital channelization filter may be changed for extracting a different desired signal from the digitized signal.

A digitised input wideband signal may be reconstructed from the digitised interference-suppressed signal and the interference cancellation signal.

The input wideband signal may be scaled to provide a scaled first signal that swings over approximately the maximum input range for the digitizing step. Alternatively, the interference-suppressed signal may be scaled to provide a scaled interference-suppressed signal that swings over approximately the maximum input range for the digitizing step.

In accordance with further aspects of the invention, apparatuses are disclosed for implementing the methods of the foregoing aspects of the invention. These and other aspects of the invention are set forth in detail hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

A small number of embodiments are described hereinafter with reference to the drawings, in which:

Fig. 1 is a block diagram of a wideband software radio receiver;

Fig. 2 is a block diagram of a system for dynamic range reduction in accordance with an embodiment of the invention;

Fig. 3 is a block diagram of another system for dynamic range reduction in accordance with an alternate embodiment of the invention;

Figs. 4(a), 4(b), and 4(c) are spectral graphs of the spectrum of signals at nodes A, B, and C, respectively, of Fig. 2;

Fig. 5 is a block diagram of a simulated system based on GSM standards;

Fig. 6 is a spectral graph of the power spectrum (dB) of a received signal of a GSM receiver;

Fig. 7 is a graph depicting a BER comparison (BER vs SNR(dB)) between a feedforward form in accordance with an embodiment of the invention and a conventional approach; and

Fig. 8 is a graph depicting a BER comparison (BER vs E_b/N_0 (dB)) between the feedforward and feedback forms in accordance with embodiments of the invention.

DETAILED DESCRIPTION

Methods and apparatuses for processing an input wideband signal containing a desired signal and a plurality of interfering signals are described hereinafter. Numerous specific details are set forth including filter types, simulation models and tools, and the like. However, it will be apparent to those skilled in the art that modifications and/or

substitutions may be made thereto without departing from the scope and spirit of the invention. In other instances, features well known to those skilled in the art have been described only briefly or omitted so as not to obscure the invention.

Fig. 2 is a block diagram depicting a dynamic range reduction technique in accordance with an embodiment of the invention. Fig. 3 depicts the technique implemented in a more compact architecture. These two architectures in accordance with embodiments of the invention are referred as the *feedforward* and *feedback* forms hereafter. For ease of description, the concept and operation of the architectures are explained mainly based on the feedforward form 200 of Fig. 2, because of its relatively straightforward architecture.

Feedforward Form

In Fig. 2, a received wideband signal 200 is input at node A to a splitter 210, which provides separate outputs to a subtractor (+ input) 212 and an automatic-gain-control (AGC) circuit 222, labelled AGC2. The spectrum of the received wideband signal 210 is depicted in Fig. 4(a). The received signal 200 consists of multiple interfering signals at different carrier frequencies whose power is much larger than a desired signal. The output of subtractor 212 is node C, which is input to another AGC circuit 214, labelled AGC1. The output of AGC1 214 is input to ADC1 216. The received signal 200 split by the splitter 210 is firstly scaled by the AGC1 214 and digitised by ADC1 216 with relatively low resolution. The scaling function of AGC1 214 ensures that the input signal of ADC1 216 occupies the full input range of the ADC1 216.

The output of ADC1 216 is coupled to a channelization filter 218 and a control input of an adaptive filter 228. The ADC1 216 can also optionally be coupled to a combiner 232. The output of the adaptive filter 228 is coupled to a digital-to-analog conversion (DAC) circuit 230 and an optionally to another input of the combiner 232. The output of DAC 230 is coupled to the subtractor (- input) 212. The channelization filter 218 and the combiner 232 provide a digitized digital signal 220 and digitized wideband signal 234, respectively.

The output of AGC2 222 is coupled to ADC2 224, which is in turn coupled to a bandstop filter 226. A channel selection module controls the bandstop filter 226 and the

channelization filter 218, with an input to each of filters 226 and 218. The output of the bandstop filter 226 is node B, which is provided to the input of the adaptive filter 228. The digitised signal produced by AGC2 222 and ADC2 224 is passed through the band-stop filter 226, which attenuates the desired signal and allows the interfering or blocking signal outside of the desired signal band to pass without attenuation. However, the filtering operation introduces phase-shift to the blocking signal as well as to the small residual desired signal, whose existence is due to the non-ideality of the band-stop filter 226. The spectrum of the filtered signal at node B is illustrated in Fig. 4(b), where diagonal-line hatching distinguishes the phase-shifted signals in Fig. 4(b) from the original signals in Fig. 4(a).

To achieve substantial spectrum subtraction and hence interfering signal suppression, the phase-shifted blocking signals have to undergo phase-correction before the blocking signals can be subtracted from the received signal. This task is carried out by the adaptive filter 228 indicated in Fig. 2. The operation of the adaptive filter 228 is elaborated hereinafter. For present purposes, the filter 228 is assumed to carry out the task effectively. Therefore, the output of the adaptive filter 228 consists mostly of the interfering signals that are almost in-phase with the original signals at node A of Fig. 2. The output signal from the filter 226 is converted into an analogue signal by a DAC 230. Having synchronous blocking signals at both inputs, the subtractor 212 results in substantial suppression of the interfering signals. Because only small residue of the desired signal lies at one of the subtractor input 212 (-input), the desired signal is not significantly affected by the subtraction. The spectrum of the signal at the output of the subtractor 212, at node C, is depicted in Fig. 4(c). AGC2 222 serves the same purpose as AGC1 216. Since the strong interfering signals are suppressed, the dynamic range requirements of ADC2 224 are consequently mitigated. Optionally, the outputs of the ADC1 216 and the adaptive filter 228 can be summed to provide the digitised wideband signal 234 for multiple channel signal processing.

Feedback Form

Like feedforward form 200 of Fig. 2, the feedback form 300 shown in Fig. 3 is able to suppress strong interfering signals by using only one set of ADC 316 and AGC 312 instead of two in the former. The received wideband signal 210 is input to an AGC

circuit 312. The output of the AGC 312 is input to a subtractor (+ input) 314. The other input of the subtractor (- input) is received from the output of a DAC circuit 326. The output of the subtractor is input to an ADC module 316. The received signal 310 is initially scaled by the AGC 312 and digitised by the ADC 314. This AGC 312 ensures that the input signal of the ADC 316 occupies the full input range of the ADC 316. The output of the ADC 316 is input to a channelization filter 320, a combiner 318, and a control input of an adaptive filter 328. The channelization filter produces a digitized desired signal 330.

The output of the combiner 318 is provided as input to the bandstop filter 322 and provides a digitized wideband signal 332 as output. The digitised signal from ADC 316 is passed through the band-stop filter 322, which only allows the interfering signals to pass without attenuation. The output of the bandstop filter 322 is provided to the adaptive filter 328. The channel selection module 324 provides a control input to each of the channelization filter 320 and the bandstop filter 322. The adaptive filter 328 provides an input to the DAC 326 and the combiner 318.

Like the feedforward form 200, the adaptive filter 328 in the feedback form 300 phase corrects the interfering signals from the band-stop filter 322. The phase-corrected interfering signals are then converted into an analogue signal by a DAC 326 before the phase-corrected interfering signals are subtracted from the incoming received signal 310 by the subtractor 314. Such a feedback loop suppresses the strong interfering signals in the wideband-received signal 310 before the wideband signal is digitised. Hence, in order to retain the statistical information of the interfering signals required by the adaptive filter 328, the reconstructed interfering signals from the adaptive filter 328 are added back to the suppressed digitised signal by the combiner 318, before being passed through the bandstop filter 322.

Since the suppressed digitised signal serves the *error function* (Simon Haykin, *Adaptive Filter Theory*, 3rd edition, Prentice Hall, 1996, pp. 370) for tuning the taps weights of the adaptive filter 328, a delay is added to align this signal with the output of the bandstop filter 322. Depending on the required signal, this feedback form can generate either the

digitised wideband signal 332, or the digitised desired signal 330 for further signal processing.

The architecture of the adaptive filter 228, 328 in Figs. 2 and 3, respectively, can be a finite-impulse-response (FIR) filter, an infinite-impulse-response (IIR) filter, or a Lattice filter. Popular algorithms such as LMS and RLS (Simon Haykin, *Adaptive Filter Theory*, 3rd edition, Prentice Hall, 1996, pp. 367-372 and 566-571) can be used to update the tap weights of the filter. The digitised output of the subtractor is used as the *error function* (Simon Haykin, *Adaptive Filter Theory*, 3rd edition, Prentice Hall, 1996, pp. 370) for tuning the tap weights of the adaptive filter. Here, using an LMS algorithm as an example, the tap-weight updating equation of the adaptive filter 228 in the feedforward form 200 shown in Fig. 2 is given as:

$$\begin{aligned}\underline{W}(n+1) &= \underline{W}(n) + \mu \cdot u(n) \cdot e(n) \\ &= \underline{W}(n) + \mu \cdot \Pi_1(r(t)) \cdot \Pi_2(r(t) - a(t)),\end{aligned}\quad (1)$$

where $\underline{W}(n)$, $u(n)$, $e(n)$ denote the vector containing the tap weights of the adaptive filter, the input of the filter, and the output of ADC1 216 at the time instant n respectively; $r(t)$ and $a(t)$ denote the received signal and the DAC 230 output; $\Pi_1(\cdot)$ and $\Pi_2(\cdot)$ represent the combined operations of AGC2 222, ADC2 224, bandstop filter 226, and the combined operations of AGC2 222 and ADC2 224, respectively. The tap-weight updating equation for the feedback form shown in Fig. 3 is similar except $\Pi_1(\cdot)$ and $\Pi_2(\cdot)$ represent different sets of operations.

The channelization filter 218, 320 in both forms 200, 300 extracts the desired signal from the input for further signal processing. Both being digital, the channelization filter 200, 300 and the band-stop filter 226, 322 can be reconfigured by the channel selection block 236, 324 to receive different channels.

Comparing Figs. 2 and 3, the feedback form 300 of the technique requires only one set of ADC and AGC. Hence, the latter has more power saving and is more suitable for mobile handset implementation. The two forms also have comparable performance. However,

the AGCs in both forms may be removed for simpler implementation, as long as the signal input to the ADC is not too small to cause significant degradation in the digitizer.

If the power levels of the desired signal and interfering signal are comparable, it may be unnecessary to employ the proposed technique and an ADC with ordinary resolution alone may be able to provide sufficient dynamic-range for the desired signal. Instead, in the case as described above, the whole system as shown in Figs. 2 and 3 may be replaced by a set of AGC and ADC without affecting the performance severely.

Simulation Results

Simulations have been carried out to evaluate the performance of the techniques in accordance with the embodiments of the invention. Simulation models have been developed on SPW[®] platform and are described hereinafter. Simulation results are also summarised.

System Model

Simulation models have been designed based on GSM standards: see *GSM 05.05 technical specifications: radio transmission and reception*, Ver. 5.8.1, October 1998, pp. 12; and *GSM 05.02 technical specifications: multiplexing and multiple access on the radio path*, Ver. 5.0.0, May 1996, pp. 22-23. The details of the designs of a GSM transmitter and receiver are described in Bjerke B.A., Proakis, J.G., Lee, K.Y.M., Zvonar Z.A., "Comparison of GSM receivers for fading multipath channels with adjacent and co-channel interference", *IEEE JSAC*, pp. 2211-2219, Vol. 18, No. 11, November 2000.

Fig. 5 is a block diagram illustrating the simulated system 500, including a GSM transmitter 510 and a GSM receiver 550. The GSM transmitter 510 includes a data source 512, GSM frame generator, a differential encoder 516, and a GMSK modulator 518, connected sequentially. The output of the GSM transmitter 510 is provided to an AWGN channel 520. The output of the channel 520 is summed using summer/combiner 530 and a signal from an interfering signal generator 540. A simple AWGN channel has been used in the simulation. The interfering signals are assumed to be GMSK modulated and have the same bandwidth as the desired signal. The interfering signals are modulated

at carrier frequencies offset from the desired channel. The output of the combiner 530 is provided to the input of the GSM receiver 550.

The GSM receiver 550 includes a digitization system for dynamic range reduction in accordance with that of Fig. 2 or Fig. 3, a downconverter 554, a phase derotation module 556, a viterbi equalizer 560, and a detector 562, connected sequentially. The output of the phase derotation module 556 is coupled to a channel estimator, which in turn is coupled to another input of the viterbi equalizer 560. The output of the GSM receiver 550 (from detector 562) is recovered data 570.

Results

Simulations have been carried out to compare the performance of the proposed digitisation technique and a conventional approach. The simulation model for the conventional approach is the same as that shown in Fig. 5 with the digitisation scheme block 552 replaced with a single ADC instead.

Case 1

Fig. 6 shows the spectrum of the signal received by the GSM receiver 500, which consists of two interfering signals located at 800kHz (-29dB) from the desired signal (-98dB), whose power spectrum density is approximately 64dB stronger than the latter.

The BER performance of the feedforward form 200 and the conventional approach is compared in Fig. 7. For both the feedforward form 200 ("Feedforward") and the conventional approach ("ADC"), the BER performance improves when ADC resolution is increased. However, for feedforward form 200, the improvement is marginal for ADC1 resolution above 10 bits. In fact, the three curves for the feedforward form 200 corresponding to ADC1 of 10, 11, and 12 bits almost overlap with each other, and with the curve corresponding to conventional approach with ADC resolution of 13 bits. This shows the employment of a dynamic range reduction technique in accordance with the embodiments of the invention results in the ADC dynamic range reduction of 3 bits, equivalent to 18 dB.

Case 2

Fig. 8 shows a comparison between the BER performance of the feedforward and feedback forms 200, 300 in accordance with the embodiments of the invention. In the feedforward form, ADC1 and ADC2 are set at 10 bits and 8 bits, respectively. In the feedback form, the ADC is set at 10 bits. The received signal consists of four interfering signals of -33dBm at 2, 2.6, 3, 3.4 MHz frequency offset from the desired signal at -99dBm . Both the feedforward and feedback forms 200, 300 have similar performance and result in the ADC dynamic range reduction of 3 bits as in Case 1.

The method for dynamic range reduction in a wideband receiver in accordance with the embodiments of the invention is a simple solution for the ADC dynamic-range problem in software radio. In addition, the technique is able to differentiate a desired signal from interfering signals by employing a bandstop filter centred at the desired carrier frequency. With this added feature, suppression of the interfering signals can be achieved, without distorting the desired signal even when the desired signal has same power as the interfering signals. Moreover, the dynamic range reduction technique in accordance with the embodiments of the invention has the flexibility of different forms of implementation depending on the hardware requirements. Another important advantage of this technique is its capability of suppressing time-varying interfering signals.

Advantageously, embodiments of the invention can adaptively suppress unwanted signals so as to reduce the dynamic-range requirement of the digitizer in a wideband receiver. Further, unlike other existing techniques, embodiments of the invention are able to differentiate a desired signal from interfering signals by employing a bandstop filter centred at the desired carrier frequency. Still further, to correct the phase-shift incurred on the interfering signals by the filtering process, an adaptive filter is used in the embodiments of the invention. Still further, suppression of the interfering signals is carried out by subtracting the phase-shifted interfering signals from the received signal. With the technique in accordance with the embodiments of the invention, suppression of the interfering signals can be achieved, without distorting the wanted signal even when the wanted signal has same power as the interfering signals. With the adaptive filter, the technique is able to suppress time-varying interfering signals. With the two forms of architecture, namely feedforward and feedback forms, this technique has the flexibility of implementing different forms of architecture depending on the hardware requirements.

In the foregoing manner, methods and apparatuses for processing an input wideband signal containing a desired signal and a plurality of interfering signals have been described. While only a small number of embodiments have been described, it will be apparent to those skilled in the art that modifications and/or substitutions may be made thereto without departing from the scope and spirit of the invention.

We claim:

1. A method for processing an input wideband signal containing a desired signal and a plurality of interfering signals, said method comprising the steps of:
 - splitting said input wideband signal into a first signal for a first signal path and a second signal for a second signal path, said first and second signals each being an analog representation of said input wideband signal;
 - digitizing said second signal to provide a digitized second signal;
 - suppressing said desired signal in said digitised second signal to provide a plurality of interference-dominant signals;
 - applying a phase shift to said plurality of interference-dominant signals to provide a plurality of digital, phase-shifted signals through said second path that is substantially the same as a phase shift through said first path;
 - converting said plurality of digital, phase-shifted signals into analog form to provide a plurality of analog regenerated signals; and
 - combining said plurality of analog regenerated signals from said second signal path and said first signal from said first signal path to provide an interference-suppressed, input wideband signal based on a difference of said plurality of analog regenerated signals and said first signal.
2. The method according to claim 1, further comprising the step of digitizing said interference-suppressed, wideband input signal to provide a digitised interference-suppressed input signal.
3. The method according to claim 2, further comprising the step of extracting said desired signal from said digitised interference-suppressed input signal.
4. The method according to claim 3, wherein said suppressing step is implemented using a digital filter and said extracting step is implemented using a channelization filter, and further comprising the step of changing coefficients of said digital filter and said digital channelization filter to extract a different desired signal from said digitised interference-suppressed input signal.

5. The method according to any one of claims 2 to 4, further comprising the step of combining said digitised interference-suppressed input signal and said plurality of digital, phase-shifted signals to provide a digitised wideband input signal.

6. The method according to any one of claims 2 to 5, further comprising the step of controlling the amplitude of said interference-suppressed, input wideband signal.

7. The method according to claim 6, wherein said interference-suppressed, input wideband signal is scaled to provide a scaled interference-suppressed, input wideband signals that swings over approximately the maximum input range of said digitizing means.

8. The method according to any one of claims 2 to 7, wherein said phase-shift applying step is implemented using a phase-shifting circuit, and further comprising the steps of receiving said digitised interference-suppressed input signal and changing coefficients of said phase shifting circuit.

9. The method according to any one of claims 1 to 7, wherein said phase-shifting applying step is implemented using an adaptive filter having coefficients that can be constantly updated using a filter-weight-updating algorithm so that variation of the characteristics of said input wideband signal is able to be tracked.

10. The method according to any one of the preceding claims, further comprising the step of making a delay through said first path equal to a delay through said second signal path.

11. The method according to any one of the preceding claims, further comprising the step of controlling the amplitude of said second signal.

12. The method according to claim 11, wherein said second signal is scaled to provide a scaled second signal that swings over approximately the maximum input range of said digitizing means.

13. An apparatus for processing an input wideband signal containing a desired signal and a plurality of interfering signals, said apparatus comprising:

a signal splitter for splitting said input wideband signal into a first signal for a first signal path and a second signal for a second signal path, said first and second signals each being an analog representation of said input wideband signal;

means for digitizing said second signal to provide a digitized second signal;

a digital filter for suppressing said desired signal in said digitised second signal to provide a plurality of interference-dominant signals;

a phase-shifting circuit for applying a phase shift to said plurality of interference-dominant signals to provide a plurality of digital, phase-shifted signals through said second path that is substantially the same as a phase shift through said first path;

means for converting said plurality of digital, phase-shifted signals into analog form to provide a plurality of analog regenerated signals; and

a signal combiner for receiving said plurality of analog regenerated signals from said second signal path and for receiving said first signal from said first signal path to provide an interference-suppressed, input wideband signal based on a difference of said plurality of analog regenerated signals and said first signal.

14. The apparatus according to claim 13, further comprising means for digitizing said interference-suppressed, wideband input signal to provide a digitised interference-suppressed input signal.

15. The apparatus according to claim 14, further comprising a digital channelization filter for extracting said desired signal from said digitised interference-suppressed input signal.

16. The apparatus according to claim 15, further comprising a channel selection circuit for changing coefficients of said digital filter and said digital channelization filter to extract a different desired signal from said digitised interference-suppressed input signal.

17. The apparatus according to any one of claims 14 to 16, further comprising a processor for receiving said digitised interference-suppressed input signal and changing coefficients of said phase shifting circuit.

18. The apparatus according to any one of claims 14 to 17, further comprising a digital combiner for receiving said digitised interference-suppressed input signal and said plurality of digital, phase-shifted signals to provide a digitised wideband input signal.

19. The apparatus according to any one of claims 14 to 18, further comprising an amplitude-scaling circuit for controlling the amplitude of said interference-suppressed, input wideband signal.

20. The apparatus according to claim 19, wherein said interference-suppressed, input wideband signal is scaled to provide a scaled interference-suppressed, input wideband signals that swings over approximately the maximum input range of said digitizing means.

21. The apparatus according to any one of claims 13 to 20, further comprising a delay in said first signal path for making a delay through said first path equal to a delay through said second signal path.

22. The apparatus according to any one of claims 13 to 21, further comprising an amplitude-scaling circuit for controlling the amplitude of said second signal.

23. The apparatus according to claim 22, wherein said second signal is scaled to provide a scaled second signal that swings over approximately the maximum input range of said digitizing means.

24. The apparatus according to any one of claims 13 to 23, wherein said phase-shifting circuit is an adaptive filter having coefficients that can be constantly updated using a filter-weight-updating algorithm so that variation of the characteristics of said input wideband signal is able to be tracked.

25. A method for processing an input wideband signal containing a desired signal and a plurality of interfering signals, said method comprising the steps of:

subtracting an analog interference cancellation signal from an input wideband signal to provide an interference-suppressed signal;

digitizing said interference-suppressed signal to provide a digitized signal;

suppressing said desired signal in said digitized signal to provide a reference interference signal;

filtering based on filter parameters said reference interference signal from said digitised signal to provide a digital interference cancellation signal; and

converting said digital interference cancellation signal into analog form to provide said analog interference cancellation signal.

26. The method according to claim 25, further comprising the step of combining said digital interference cancellation signal and said digitized signal after cancellation to provide a reconstructed digitized signal for input to said suppressing step.

27. The method according to claim 25 or 26, further comprising the step of making a delay in a signal path for said interference-suppressed signal equal to a delay through a signal path for said reference interference signal from said suppressing step.

28. The method according to any one of claims 25 to 27, further comprising the step of extracting said desired signal from said digitised interference-suppressed signal.

29. The method according to claim 28, wherein said suppressing step is implemented using a digital filter and said extracting step is implemented using a digital channelization filter, and further comprising the step of changing coefficients of said digital filter and said digital channelization filter for extracting a different desired signal from said digitized signal.

30. The method according to any one of claims 25 to 29, further comprising the step of reconstructing a digitised input wideband signal from said digitised interference-suppressed signal and said interference cancellation signal.

31. The method according to any one of claims 25 to 30, further comprising the step of scaling said input wideband signal to provide a scaled first signal that swings over approximately the maximum input range for said digitizing step.

32. The method according to any one of claims 25 to 31, further comprising the step of scaling said interference-suppressed signal to provide a scaled interference-suppressed signal that swings over approximately the maximum input range for said digitizing step.

33. An apparatus for processing an input wideband signal containing a desired signal and a plurality of interfering signals, said apparatus comprising:

a subtractor for subtracting an analog interference cancellation signal from an input wideband signal to provide an interference-suppressed signal;

means for digitizing said interference-suppressed signal to provide a digitized signal;

a digital filter for suppressing said desired signal in said digitized signal to provide a reference interference signal;

an adaptive filter for filtering based on filter parameters said reference interference signal from said digitised signal to provide a digital interference cancellation signal;

means for converting said digital interference cancellation signal into analog form to provide said analog interference cancellation signal.

34. The apparatus according to claim 33, further comprising a signal combiner for combining said digital interference cancellation signal and said digitized signal after cancellation from said digitizing means to provide a reconstructed digitized signal for input to said digital filter.

35. The apparatus according to claim 33 or 34, further comprising means for making a delay in a signal path for said interference-suppressed signal equal to a delay through a signal path for said reference interference signal from said digital filter.

36. The apparatus according to any one of claims 33 to 35, further comprising a digital channelization filter for extracting said desired signal from said digitised interference-suppressed signal.

37. The apparatus according to claim 36, further comprising a channel selection circuit for changing coefficients of said digital filter and digital channelization filter for extracting a different desired signal from said digitized signal.

38. The apparatus according to any one of claims 33 to 37, further comprising a digital combiner to reconstruct a digitised input wideband signal from said digitised interference-suppressed signal and said interference cancellation signal.

39. The apparatus according to any one of claims 33 to 38, further comprising means for scaling said input wideband signal to provide a scaled first signal that swings over approximately the maximum input range of said digitizing means.

40. The apparatus according to any one of claims 33 to 39, further comprising means for scaling said interference-suppressed signal to provide a scaled interference-suppressed signal that swings over approximately the maximum input range of said digitizing means.