

ABSTRACT

A HIGH VOLTAGE TOLERANT ESD DESIGN FOR ANALOG AND RF APPLICATIONS IN DEEP SUBMICRON CMOS TECHNOLOGIES

The invention describes structures and a process for providing ESD semiconductor protection with reduced input capacitance which has special advantages for high frequency analog pin I/O applications. The structures consist of a first and second NMOS serial pair whose capacitance is shielded from the I/O pin by a serial diode. The first serial pair provide an ESD voltage clamp between the I/O pin and the Vcc voltage source. The second pair provides an ESD voltage clamp between the I/O pin and Vss, or ground voltage source. The triggering of both pairs is enhanced by a NMOS device whose gate is dynamically coupled to the ESD energy through capacitance and a RC network. The serial pairs can be used separately to match specific application requirements or used together,

(Fig. 3A)



G00002



162162