CLAIMS

WHAT IS CLAIMED IS:

1. A memory system, comprising:

an interface and a controller, wherein the interface is configured to perform operations comprising:

receiving, from a host, commands; and

sending, to the host at a time instant, responses, each of the responses is generated in the memory system during a time period and responsive to a respective one of the commands.

2. The memory system according to claim 1, wherein the controller is coupled to the interface and configured to perform one or more operations comprising:

receiving, through the interface, the commands from the host; and

in response to receiving the commands, generating the responses.

3. The memory system according to claim 1, wherein the time instant for sending the responses is after the time period in response to determining that the time period is longer than or equal to a predetermined time period.

4. The memory system according to claim 1, wherein the time instant for sending the responses is during the time period in response to determining that a quantity of the responses generated is greater than or equal to a predetermined threshold.

5. The memory system according to claim 1, wherein the commands comprise random read or write commands, and wherein a size of each of the random read or write commands is less than or equal to 4kb.

6. The memory system according to claim 1, wherein the memory system comprises a universal flash storage (UFS) device, and wherein the UFS device comprises the controller and a memory device.

7. The memory system according to claim 6, wherein a respective data structure of each read command in the commands comprises a read command UFS protocol information unit (UPIU), a respective data structure of each write command in the commands comprises a write command UPIU, a respective data structure of each read response in the responses comprises a read response UPIU, and a respective data structure of each write response in the responses comprises a write response UPIU.

8. A memory system, comprising:

a memory device and a controller coupled to the memory device, wherein the controller is configured to perform operations comprising:

receiving, from a host, commands;

in response to receiving the commands, generating, during a time period, responses, each of the responses is responsive to a respective one of the commands; and

sending, at a time instant, the generated responses to the host.

9. The memory system according to claim 8, wherein the time instant for sending the responses is after the time period in response to determining that the time period is longer than or equal to a predetermined time period.

10. The memory system according to claim 8, wherein the time instant for sending the responses is during the time period in response to determining that a quantity of the responses generated is greater than or equal to a predetermined threshold.

11. The memory system according to claim 8, wherein the commands comprise random read or write commands, and wherein a size of each of the random read or write commands is less than or equal to 4kb.

12. The memory system according to claim 8, wherein the memory system comprises a universal flash storage (UFS) device, and wherein the UFS device comprises the controller and the memory device.

13. The memory system according to claim 12, a respective data structure of each read command in the commands comprises a read command UFS protocol information unit (UPIU), a respective data structure of each write command in the commands comprises a write command UPIU, a respective data structure of each read response in the responses comprises a read response UPIU, and a respective data structure of each write response in the responses comprises a write response UPIU.

14. The memory system according to claim 10, wherein the operations further comprise:

receiving a state of a response counting switch;

receiving a predetermined threshold value; and

receiving a predetermined time period value.

15. The memory system according to claim 14, wherein the operations further comprise:

determining that the received state of the response counting switch is on;

determining that an auto-response switch is on; and

in response to determining that the state of the response counting switch is on and that the auto-response switch is on:

turning off the auto-response switch;

setting the predetermined threshold to be the received predetermined threshold value; and

setting the predetermined time period to be the received predetermined time period value.

16. A method of controlling a memory system, the method comprising:

receiving, from a host, commands; and

sending, to the host at a time instant, responses, each of the responses is generated in the memory system during a time period and responsive to a respective one of the commands.

17. The method according to claim 16, wherein the time instant for sending the responses is after the time period in response to determining that the time period is longer than or equal to a predetermined time period.

18. The method according to claim 16, wherein the time instant for sending the responses is during the time period in response to determining that a quantity of the responses generated is greater than or equal to a predetermined threshold.

19. The method according to claim 16, wherein the commands comprise random read or write commands, and wherein a size of each of the random read or write commands is less than or equal to 4kb.

20. The method according to claim 16, wherein the memory system comprises a universal flash storage (UFS) device, and wherein the UFS device comprises a controller and one or more memory devices.