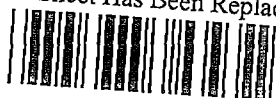


ABSTRACT OF THE DISCLOSURE

A sense amplifier, which is intended to reduce the output response time after it has received a small voltage difference until it delivers amplified output signals, consists of a latch circuit made up of a pair of CMOS inverters, a pair of NMOS transistors connected in parallel to the latch circuit, and a current source connected in series to the latch circuit and NMOS transistor pair. The NMOS transistors amplify a small voltage difference of input signals, and the inverters of the latch circuit further amplify the resulting voltage difference to produce the output signals. Based on that a small voltage difference of input signals is amplified in two stages and that the amplifying circuit is of 2-stage serial connection of the current source and the NMOS transistor or CMOS inverter, the delay time of output response can be reduced.

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