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The diagram illustrates a video signal processing system, specifically an equalizer (50) and its associated components. The system is divided into several functional blocks:

- Input and Initial Processing:** The signal enters through a **TUNER** (14), followed by **DEMOD. AND CARRIER RECOVERY** (18), and an **ADC** (19).
- Field Sync Detection:** A **FIELD SYNC DETECTOR** (17) receives the signal and outputs a **FIELD SYNC DETECT** signal.
- Equalizer (50):** This central block contains:
  - SEG. SYNC AND CLOCK RECOVERY** (15): Receives the signal and outputs **SEG. SYNC DETECT** and **CONTROL** signals.
  - PN REF. SEQUENCE FROM 70, 66**: Provides a reference signal to a **MUX** (29) and a **LEVEL SLICER** (40).
  - MUX** (29): A 2-to-1 multiplexer controlled by **CONTROL** signals, outputting the **EQUALIZER OUTPUT**.
  - LEVEL SLICER** (40): Receives the equalizer output and provides **CONTROL** feedback.
  - CMA** (25): A Constant Modulus Algorithm block that receives the equalizer output and provides **CONTROL** feedback.
  - MUX** (26): A 2-to-1 multiplexer controlled by **CONTROL** signals, outputting **COEFFICIENT CONTROL** to a **DFF** (28).
  - DFF** (28): A Digital Flip-Flop that outputs **CONTROL** signals to the **MUX** (29) and **MUX** (26).
  - FF** (20): A Feed-Forward block that receives the equalizer output and provides **CONTROL** feedback.
  - +** (24): A summing junction that combines the equalizer output with the output of the **FF** (20) block.
- Control and Memory:** A **CONTROL SIGNAL GENERATOR** (66) receives **SEG. SYNC DETECT** and **FIELD SYNC DETECT** signals. It outputs **CONTROL** signals to the **MUX** (29) and **MUX** (26), and a **PN REFERENCE** signal to the **PN REF. SEQUENCE FROM 70, 66** block. It also interfaces with **MEMORY** (70).
- Output Stage:** The equalizer output is processed by a **DECODER** (60) and an **OUTPUT PROCESSOR** (64) to produce the final output.

An adaptive channel equalizer (50) for processing a demodulated VSB signal containing terrestrial broadcast high definition television information includes an adaptive feed forward filter (FFF 20) and an adaptive decision feedback filter (DFF 30). The equalizer is preceded by a demodulator/carrier recovery network (18) and does not include a carrier recovery function in the equalizer control loop. The equalizer FFF and DFF elements operate adaptively in blind, training, and decision-directed modes. A direct connection provided from the equalizer output to the DFF facilitates coarse signal acquisition and equalization during the blind operating mode.