(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 May 2002 (10.05.2002)

PCT

(10) International Publication Number
WO 02/037552 A3

(51) International Patent Classification[7]: H01L 21/336, 29/788

(21) International Application Number: PCT/US01/46127

(22) International Filing Date: 30 October 2001 (30.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/699,711 30 October 2000 (30.10.2000) US
60/291,859 18 May 2001 (18.05.2001) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

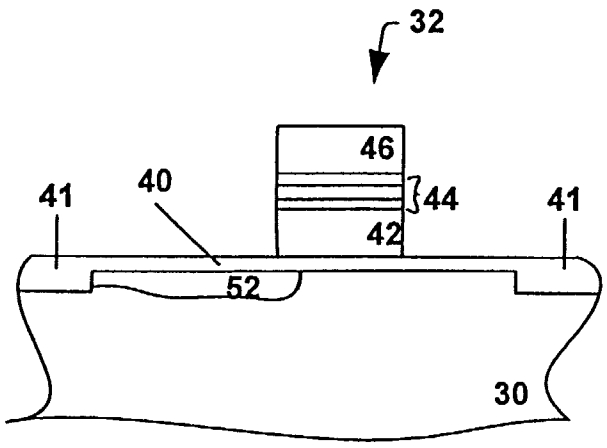
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*

(88) Date of publication of the international search report:
13 March 2003

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: DOPING FOR FLASH MEMORY CELL




(57) Abstract: For fabricating a flash memory cell on a semiconductor substrate, a channel dopant is implanted into the semiconductor substrate. The concentration of the channel dopang in the semiconductor substrate from the implantation process is less than about $4X10^{13}/Cm^2$. A source line mask is formed over the substrate, and the source link mask has an opening to expose a source line of the semiconductor substrate. A source line dopant of a first conductivity type is implanted into the exposed source line of the semiconductor substrate. The source line mask is then removed from the semiconductor substrate. A drain mask is formed over the semiconductor substrate, and the drain mask has an opening to expose a drain region of the semiconductor substrate. A drain dopant of a second conductivity type is implanted into the exposed drain region of the semiconductor substrate. A channel region of the semiconductor substrate is disposed between the source line and the drain region. The first conductivity type of the source line dopant is opposite to the second conductivity type of the drain dopang. In addition, a conductivity type of the channel dopant is same as the first conductivity type of the source line dopant. The source line dopant that diffuses from the source line into the channel region is used to alter a threshold voltage of the flash memory cell and/or to reduce short channel effects of the flash memory cell such that a lower concentration of the channel dopant is implanted or such that the implantation of the channel dopant is even eliminated, for improved reliability and performance of the flash memory cell.

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