~~WHAT IS CLAIMED IS:~~

1. A circuit comprising:

a first domain comprising a first power clamp coupled to a first power rail and a first ground rail, and a first interface connection configured to transmit signals from the first domain;

a second domain comprising a second power clamp coupled to a second power rail and a second ground rail, and a second interface connection configured to receive signals into the second domain; and

a blocking circuit for blocking current from an ESD event, the blocking circuit having an input connection coupled to the first interface connection and an output connection coupled to the second interface connection.

2. The circuit according to claim 1, wherein the blocking circuit comprises:

a first NMOS having a first NMOS gate, a first NMOS drain, and a first NMOS source coupled to the first ground rail;

a second NMOS having a second NMOS gate, a second NMOS drain, and a second NMOS source coupled to the first ground rail; and

an inverter having an input coupled to the input connection and the first NMOS gate, and having an output coupled to the second NMOS gate.

3. The circuit according to claim 2, wherein the blocking circuit further comprises:

a first core PMOS having a first core PMOS gate, a first core PMOS drain, and a first core PMOS source coupled to the second power rail; and

a second core PMOS having a second core PMOS gate, a second core PMOS drain, and a second core PMOS source coupled to the second power rail, wherein the first NMOS drain is coupled to the first core PMOS drain and the second core PMOS gate, and wherein the output connection is coupled to the second core PMOS drain, the second NMOS drain, and the first core PMOS gate.

4. The circuit according to claim 2, wherein the second domain further comprises a core PMOS having a core PMOS gate, a core PMOS drain, and a core PMOS source coupled to the second power rail; and a core NMOS having a core NMOS gate coupled to the core PMOS gate and the second interface connection, a core NMOS drain coupled to the core PMOS drain, and a core NMOS source coupled to the second ground rail, wherein the first NMOS and the inverter have a gate oxide breakdown voltage greater than a gate oxide breakdown voltage of the core PMOS and the core NMOS, and wherein the first power rail has a voltage greater than the second power rail.

5. The circuit according to claim 4, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5 volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

6. The circuit according to claim 1, further comprising:

a first RC clamp coupled to the first power rail and the first ground rail; and

a diode having an anode coupled to the first ground rail and a cathode coupled to the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode.

7. The circuit according to claim 6, further comprising a second RC clamp coupled to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

8. The circuit according to claim 1, wherein no leakage current from the first power rail to the second power rail flows through the blocking circuit when the first power rail is energized before the second power rail.

9. A method comprising:

coupling a first power clamp to a first power rail and a first ground rail of a first domain;

coupling a second power clamp to a second power rail and a second ground rail of a second domain;

providing a blocking circuit for blocking current from an ESD event;

providing an I/O interface connection in the first domain for transmitting signals from the first domain to the blocking circuit;

providing a core interface connection in the second domain for transmitting signals from the blocking circuit to the second domain;

coupling an input connection of the blocking circuit to the I/O interface connection; and

coupling an output connection of the blocking circuit to a core interface connection.

10. The method according to claim 9, further comprising:

providing in the blocking circuit a first NMOS transistor having a first NMOS source, a first NMOS drain, and a first NMOS gate;

coupling the first NMOS source to the first ground rail;

providing in the blocking circuit a second NMOS transistor having a second NMOS source, a second NMOS drain, and a second NMOS gate;

coupling the second NMOS source to the first ground rail;

providing an inverter in the blocking circuit;

coupling an output of the inverter to the second NMOS gate; and

coupling an input of the inverter to the first NMOS gate and the input connection.

11. The method according to claim 10, further comprising:

providing in the blocking circuit a first core PMOS transistor having a first core PMOS source, a first core PMOS drain, and a first core PMOS gate;

coupling the first core PMOS source to the second power rail;

providing in the blocking circuit a second core PMOS transistor having a second core PMOS source, a second core PMOS drain, and a second core PMOS gate;

coupling the second core PMOS source to the second power rail;

coupling the first NMOS drain to the first core PMOS drain, and to the second core PMOS gate; and

coupling the second NMOS drain to the second core PMOS drain, the first core PMOS gate, and to the output connection.

12. The method according to claim 10, further comprising:

providing in the second domain a core PMOS transistor having a core PMOS source, a core PMOS drain, and a core PMOS gate, the core PMOS transistor having a gate oxide breakdown voltage less than a gate oxide breakdown voltage of the first NMOS and of the inverter;

coupling the core PMOS source to the second power rail;

providing in the second domain a core NMOS transistor having a core NMOS source, a core NMOS drain, and a core NMOS gate, the core NMOS transistor having a gate oxide breakdown voltage less than the gate oxide breakdown voltage of the first NMOS and of the inverter;

coupling the core NMOS source to the second ground rail;

coupling the core NMOS gate, the core NMOS gate and the output connection; and

coupling the core NMOS drain to the core NMOS drain, wherein the first power rail has a voltage greater than the second power rail.

13. The method according to claim 12, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5 volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

14. The method according to claim 9, further comprising:

providing a first RC clamp in the first domain for discharging current from an ESD event;

coupling the first RC clamp to the first power rail and the first ground rail;

providing a diode having an anode and a cathode connection;

coupling the anode connection to the first ground rail; and

coupling the cathode connection to the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode.

15. The method according to claim 14, further comprising:

providing a second RC clamp in the second domain for discharging current from an ESD event; and

coupling the second RC clamp to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

16. The method according to claim 9, wherein no leakage current from the first power rail to the second power rail flows through the blocking circuit when the first power rail is energized before the second power rail.

17. A circuit comprising:

a first domain comprising a first power clamp coupled to a first power rail and a first ground rail, and an I/O interface connection for sending signals from the first domain;

a second domain comprising:

a second power clamp coupled to a second power rail and a second ground rail;

a core interface connection for transmitting signals to the second domain;

a first core PMOS having a first core PMOS gate, a first core PMOS drain, and a first core PMOS source coupled to the second power rail; and

a core NMOS having a core NMOS gate coupled to the first core PMOS gate and the core interface connection, a core NMOS drain coupled to the first core PMOS drain, and a core NMOS source coupled to the second ground rail; and

a blocking circuit configured to block current from an ESD event having an input connection coupled to the I/O interface connection and an output connection coupled to the core interface connection, the blocking circuit comprising:

a first NMOS having a first NMOS gate, a first NMOS drain, and a first NMOS source coupled to the first ground rail;

a second NMOS having a second NMOS gate, a second NMOS drain, and a second NMOS source coupled to the first ground rail, wherein the input connection is coupled to the first NMOS gate, and to the second NMOS gate via an inverter, wherein the first NMOS and the inverter have a gate oxide breakdown voltage greater than a gate oxide breakdown voltage of the first core PMOS and the core NMOS;

a second core PMOS having a second core PMOS gate, a second core PMOS drain, and a second core PMOS source coupled to the second power rail; and

a third core PMOS having a third core PMOS gate, a third core PMOS drain, and a third core PMOS source coupled to the second power rail, wherein the first NMOS drain is coupled to the second core PMOS drain, and the third core PMOS gate, and wherein the output connection is coupled to the third core PMOS drain, the second NMOS drain, and the second core PMOS gate.

18. The circuit according to claim 17, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the first core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5

volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

19. The circuit according to claim 17, further comprising a diode having an anode coupled to the first ground rail and a cathode coupled to the second ground rail, wherein the first domain further comprises a first RC clamp coupled to the first power rail and the first ground rail, wherein the second domain further comprises a second RC clamp coupled to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode or on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

20. The circuit according to claim 17, wherein no leakage current from the first power rail to the second power rail flows through the I/O and core interface connections when the first power rail is energized before the second power rail.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a first domain comprising a first power clamp coupled to a first power rail and a first ground rail, and a first interface connection configured to transmit signals from the first domain;

a second domain comprising a second power clamp coupled to a second power rail and a second ground rail, and a second interface connection configured to receive signals into the second domain; and

a blocking circuit for blocking current from an ESD event, the blocking circuit having an input connection coupled to the first interface connection and an output connection coupled to the second interface connection, wherein the blocking circuit comprises a first NMOS having a first NMOS gate coupled to the input connection, a first NMOS drain, and a first NMOS source coupled to the first ground rail.

2. The circuit according to claim 1, wherein the blocking circuit further comprises:

a second NMOS having a second NMOS gate, a second NMOS drain, and a second NMOS source coupled to the first ground rail; and

an inverter having an input coupled to the input connection and the first NMOS gate, and having an output coupled to the second NMOS gate.

3. The circuit according to claim 2, wherein the blocking circuit further comprises:

a first core PMOS having a first core PMOS gate, a first core PMOS drain, and a first core PMOS source coupled to the second power rail; and

a second core PMOS having a second core PMOS gate, a second core PMOS drain, and a second core PMOS source coupled to the second power rail, wherein the first NMOS drain is coupled to the first core PMOS drain and the second core PMOS gate, and wherein the output connection is coupled to the second core PMOS drain, the second NMOS drain, and the first core PMOS gate.

4. The circuit according to claim 2, wherein the second domain further comprises a core PMOS having a core PMOS gate, a core PMOS drain, and a core PMOS source coupled to the second power rail; and a core NMOS having a core NMOS gate coupled to the core PMOS gate and the second interface connection, a core NMOS drain coupled to the core PMOS drain, and a core NMOS source coupled to the second ground rail, wherein the first NMOS and the inverter have a gate oxide breakdown voltage greater than a gate oxide breakdown voltage of the core PMOS and the core NMOS, and wherein the first power rail has a voltage greater than the second power rail.

5. The circuit according to claim 4, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5 volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

6. The circuit according to claim 1, further comprising:

a first RC clamp coupled to the first power rail and the first ground rail; and

a diode having an anode coupled to the first ground rail and a cathode coupled to the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode.

7. The circuit according to claim 6, further comprising a second RC clamp coupled to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

8. The circuit according to claim 1, wherein no leakage current from the first power rail to the second power rail flows through the blocking circuit when the first power rail is energized before the second power rail.

9. A method comprising:

coupling a first power clamp to a first power rail and a first ground rail of a first domain;

coupling a second power clamp to a second power rail and a second ground rail of a second domain;

providing a blocking circuit for blocking current from an ESD event;

providing in the blocking circuit a first NMOS transistor having a first NMOS source, a first NMOS drain, and a first NMOS gate;

coupling the first NMOS source to the first ground rail;

providing an I/O interface connection in the first domain for transmitting signals from the first domain to the blocking circuit;

providing a core interface connection in the second domain for transmitting signals from the blocking circuit to the second domain;

coupling an input connection of the blocking circuit to the I/O interface connection;

coupling the first NMOS gate to the input connection; and

coupling an output connection of the blocking circuit to a core interface connection.

10. The method according to claim 9, further comprising:

providing in the blocking circuit a second NMOS transistor having a second NMOS source, a second NMOS drain, and a second NMOS gate;

coupling the second NMOS source to the first ground rail;

providing an inverter in the blocking circuit;

coupling an output of the inverter to the second NMOS gate; and

coupling an input of the inverter to the first NMOS gate and the input connection.

11. The method according to claim 10, further comprising:

providing in the blocking circuit a first core PMOS transistor having a first core PMOS source, a first core PMOS drain, and a first core PMOS gate;

coupling the first core PMOS source to the second power rail;

providing in the blocking circuit a second core PMOS transistor having a second core PMOS source, a second core PMOS drain, and a second core PMOS gate;

coupling the second core PMOS source to the second power rail;

coupling the first NMOS drain to the first core PMOS drain, and to the second core PMOS gate; and

coupling the second NMOS drain to the second core PMOS drain, the first core PMOS gate, and to the output connection.

12. The method according to claim 10, further comprising:

providing in the second domain a core PMOS transistor having a core PMOS source, a core PMOS drain, and a core PMOS gate, the core PMOS transistor having a gate oxide breakdown voltage less than a gate oxide breakdown voltage of the first NMOS and of the inverter;

coupling the core PMOS source to the second power rail;

providing in the second domain a core NMOS transistor having a core NMOS source, a core NMOS drain, and a core NMOS gate, the core NMOS transistor having a gate oxide breakdown voltage less than the gate oxide breakdown voltage of the first NMOS and of the inverter;

coupling the core NMOS source to the second ground rail;

coupling the core NMOS gate, the core NMOS gate and the output connection; and

coupling the core NMOS drain to the core NMOS drain, wherein the first power rail has a voltage greater than the second power rail.

13. The method according to claim 12, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5 volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

14. The method according to claim 9, further comprising:

providing a first RC clamp in the first domain for discharging current from an ESD event;

coupling the first RC clamp to the first power rail and the first ground rail;

providing a diode having an anode and a cathode connection;

coupling the anode connection to the first ground rail; and

coupling the cathode connection to the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode.

15. The method according to claim 14, further comprising:

providing a second RC clamp in the second domain for discharging current from an ESD event; and

coupling the second RC clamp to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

16. The method according to claim 9, wherein no leakage current from the first power rail to the second power rail flows through the blocking circuit when the first power rail is energized before the second power rail.

17. A circuit comprising:

a first domain comprising a first power clamp coupled to a first power rail and a first ground rail, and an I/O interface connection for sending signals from the first domain;

a second domain comprising:

a second power clamp coupled to a second power rail and a second ground rail;

a core interface connection for transmitting signals to the second domain;

a first core PMOS having a first core PMOS gate, a first core PMOS drain, and a first core PMOS source coupled to the second power rail; and

a core NMOS having a core NMOS gate coupled to the first core PMOS gate and the core interface connection, a core NMOS drain coupled to the first core PMOS drain, and a core NMOS source coupled to the second ground rail; and

a blocking circuit configured to block current from an ESD event having an input connection coupled to the I/O interface connection and an output connection coupled to the core interface connection, the blocking circuit comprising:

a first NMOS having a first NMOS gate, a first NMOS drain, and a first NMOS source coupled to the first ground rail;

a second NMOS having a second NMOS gate, a second NMOS drain, and a second NMOS source coupled to the first ground rail, wherein the input connection is coupled to the first NMOS gate, and to the second NMOS gate via an inverter, wherein the first NMOS and the inverter have a gate oxide breakdown voltage greater than a gate oxide breakdown voltage of the first core PMOS and the core NMOS;

a second core PMOS having a second core PMOS gate, a second core PMOS drain, and a second core PMOS source coupled to the second power rail; and

a third core PMOS having a third core PMOS gate, a third core PMOS drain, and a third core PMOS source coupled to the second power rail, wherein the first NMOS drain is coupled to the second core PMOS drain, and the third core PMOS gate, and wherein

the output connection is coupled to the third core PMOS drain, the second NMOS drain, and the second core PMOS gate.

18. The circuit according to claim 17, wherein the first NMOS and the inverter have a gate oxide breakdown voltage of between 7 volts and 8 volts, and the first core PMOS and the core NMOS have a gate oxide breakdown voltage of between 4 volts and 5 volts and between 3.5 volts and 4.5 volts, respectively, and wherein the first power rail has a voltage of 1.65 volts to 2 volts and the second power rail has a voltage of 0.8 volts to 1 volt.

19. The circuit according to claim 17, further comprising a diode having an anode coupled to the first ground rail and a cathode coupled to the second ground rail, wherein the first domain further comprises a first RC clamp coupled to the first power rail and the first ground rail, wherein the second domain further comprises a second RC clamp coupled to the second power rail and the second ground rail, wherein current from an ESD event is discharged on a path from the first power rail to the second ground rail via the first RC clamp and the diode or on a path from the first power rail to the second power rail via the first RC clamp, the diode, and the second RC clamp.

20. The circuit according to claim 17, wherein no leakage current from the first power rail to the second power rail flows through the I/O and core interface connections when the first power rail is energized before the second power rail.