CONTROLLED-SHAPED SOLDER RESERVOIRS FOR INCREASING THE VOLUME OF SOLDER BUMPS, AND STRUCTURES FORMED THEREBY

FIELD OF THE INVENTION

This invention relates to the field of microelectronic devices, and more particularly. to solder bumps for microelectronic devices.

BACKGROUND OF THE INVENTION

High performance microelectronic devices often use solder balls or solder bumps for electrical and mechanical interconnection to other microelectronic devices. For example, a very large scale integration (VLSI) chip may be electrically connected to a circuit board or other next level packaging substrate using solder balls or solder bumps. This connection technology is also referred to as "Controlled Collapse Chip Connection - C4" or "flip-chip" technology, and will be referred to herein as "solder bumps".

A significant advance in this technology is disclosed in U. S. Patent No. 5,162,257 to Yung entitled "Solder Bump Fabrication Method" and assigned to the assignee of the present invention. In this patent, an under bump metallurgy is formed on the microelectronic substrate including contact pads, and solder bumps are formed on the under bump metallurgy opposite the contact pads. The under bump metallurgy between the solder bumps and the contact pads is converted to an intermetallic which is resistant to etchants used to etch the under bump metallurgy between solder bumps. Accordingly, the base of the solder bumps is preserved.

In many circumstances, it may be desired to provide a solder bump on the substrate at a location remote from the contact pad and also form an electrical connection between the contact pad and the solder bump. For example, a microelectronic substrate may be initially designed for wire bonding with the contact pads arranged around the outer edge of the substrate. At a later time it may

be desired to use the microelectronic substrate in an application requiring solder bumps to be placed in the interior of the substrate. In order to achieve the placement of a solder bump on the interior of the substrate away from the respective contact pad, an interconnection or redistribution routing conductor may be necessary.

U. S. Patent No. 5,327,013 to Moore et al. entitled "Solder Bumping of Integrated Circuit Die" discloses a method for forming a redistribution routing conductor and solder bump on an integrated circuit die. This method includes forming a terminal of an electrically conductive, solder-wettable composite material. The terminal includes a bond pad overlying the passivation layer remote from a metal contact and a runner that extends from the pad to the metal contact. A body of solder is reflowed onto the bond pad to form a bump bonded to the pad and electrically coupled through the runner.

In this method, however, the solder bump is formed by pressing a microsphere of a solder alloy onto the bond pad. In addition, the spread of solder along the runner during reflow is limited. In the illustrated embodiment, a solder stop formed of a polymeric solder resist material is applied to the runner to confine the solder to the bond pad.

In many circumstances, it is desirable to form relatively tall solder bumps. For example, taller solder bumps provide a larger opening between a microelectronic chip and substrate in a flip-chip module, which facilitates improved cleaning and underfill. In addition, it is generally excepted that taller solder bumps are more reliable because the straining per unit length is proportionally reduced with the increase in bump height.

A known technique for increasing solder bump height is to increase the volume solder with the same diameter solder pad. However, this technique typically requires more space on the substrate for plating or depositing the additional solder, and/or requires additional process steps. As a consequence, the benefit of increasing the bump height is often offset, at least in part, by the increase in surface area required for a single bump, and or, the additional cost associated

with providing additional solder. Other methods of decreasing the strain per unit length in the solder includes casting pillars, posts, or beams of high melting point solder and attaching these to the semiconductor using lower temperature solders.

Notwithstanding the above mentioned references, there continues to exist a need in the art for solder bump structures that are relatively tall, do not require additional surface area, and can be fabricated efficiently and at a reduced cost.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved solder bump structure.

It is another object of the present invention to provide solder bump structure with a solder redistribution reservoir for increasing the volume, and thus the height, of the solder bump.

It is another object of the present invention to provide an improved vacuum in a sealed chamber including a microelectronic device.

These and other objects are provided, according to the present invention, by a controlled-shaped solder reservoir which provides additional solder to a bump in the reflow step for increasing the volume of solder forming the solder bump. The controlled shaped reservoirs can be shaped and sized to provide predetermined amounts of solder to the solder bump. Thus, the height of the resulting solder bump can be predetermined, not to mention that the height is greater than that of similar solder bumps without solder redistribution reservoirs because of the additional solder volume added by the reservoirs. To accommodate the stringent space requirement in many microelectronic chip designs, the solder reservoir can be shaped to take a minimum amount of space. Consequently, the solder bumps may have increased height without adding to the space requirements of the solder bump, or without increasing the cost.

Other advantages of the solder structures formed in accordance with the present invention include an increase opening or gap in a flip-chip structure because of the taller solder bumps. This allows for more efficient cleaning of flux and other residues, and more efficient underfilling. The taller solder bumps can

also be utilized in conjunction with electrical contact bumps that do not have solder reservoirs so that the contact bumps are elongated by the relatively larger bumps formed with the assistance of the additional solder from the reservoirs. Consequently, the contact bumps are more reliable because the strain is distributed over a greater length (*i.e.*, height) because of the relatively larger volume bumps. Yet another advantage is that the relatively taller solder bumps can be utilized to increase the volume, and thus reduce the pressure, of a sealed chamber in a MEMS vacuum package. This enables a lower pressure vacuum environment to the generated without the equipment typically needed to generate such low pressures vacuums. Further, a single masking step can be used to define both the solder bump structure, including the solder redistribution reservoir, and the under bump metallurgy layer.

In accordance with one embodiment of the present invention, a solder structure on a microelectronic substrate comprises a solder reservoir portion and a solder bump portion, and wherein the solder reservoir portion is non-linear in shape. The solder reservoir portion may wrap around the solder bump portion in order to take up less space. In addition, the solder structure may comprise a plurality of solder reservoir portions extending from the solder bump portion. Preferably, the radially extending solder reservoirs are of substantially equal length, though the reservoirs can be of varying lengths.

In accordance with another aspect of the invention, the solder reservoir portion includes a first linear portion and a second linear portion, each having at least one straight side, and wherein a straight side of said first linear portion forms an obtuse angle with respect to a straight side of said second linear portion. Further, the solder reservoir portion may be shaped to create a pressure gradient along the length of the solder reservoir portion during a solder reflow process. Accordingly, the rate of solder flow can be controlled, which may be highly desirable in particular circumstances. The pressure gradient may increase the flow rate of solder to the solder bump portion, or the pressure gradient may decrease the flow rate of solder to the solder bump portion.

In order to reduce the area taken by the solder bump structure, the solder

reservoir portion may include a notch for facilitating the removal of the residual solder of the solder reservoir portion subsequent to the solder reflow process. The removal of the residual solder may be further facilitated by the use of high-lead solders which may facilitate the incomplete conversion of copper in the under bump metallurgy. Thus, the remaining copper may be dissolved in the subsequent etch step, thereby allowing the residual solder of the reservoir to break off at the weak point created by the notch, and float away in the etchant.

In accordance with another aspect of the present invention, a solder structure on a microelectronic substrate comprises a solder reservoir portion and a solder bump portion, and wherein the solder reservoir portion has a width which is non-uniform in at least a portion of the reservoir portion. Accordingly, a pressure gradient can be achieved within the solder reservoir to either increase or decrease the flow rate of the solder to the bump structure during the solder flow process. As mentioned above, controlling the flow rate of the solder in the solder flow process may be desirable in certain applications.

In accordance with yet another aspect of the present invention, a microelectromechanical system (MEMS) module comprises a substrate and a lid in spaced apart relationship, a solder ring which bonds the lid to the substrate to define a sealed chamber therebetween, wherein the solder ring includes at least one solder reservoir associated therewith. In addition, the device includes a MEMS device formed in the chamber.

A second solder ring that is concentrically aligned with the first solder ring may be included, wherein the second solder ring also includes at least one solder reservoir associated therewith. The MEMS module may further comprise elongated electrical contacts within the chamber, wherein the elongated electrical contacts electrically connect the lid to the substrate. Preferably, the chamber is a controlled environment maintained at a vacuum.

In accordance with another aspect of the present invention, a flip-chip structure comprises a substrate and a chip in spaced apart relationship, an elongated contact bump which electrically connects the lid to the substrate, and a plurality of mechanical bumps bonding the chip to the substrate, wherein the

mechanical bumps include solder reservoirs associated therewith. The solder reservoirs associated with the mechanical bumps may be non-linear, and may have a non-uniform width portion, as discussed above.

According to one embodiment of the present invention, there is disclosed a solder bump structure on a microelectronic substrate, comprising a solder structure including a solder reservoir portion and a solder bump portion, and wherein the solder reservoir portion comprises a first linear segment, wherein the first linear segment has opposed sides, and a second linear segment, wherein the second linear segment has opposed sides, wherein at least one side of the first linear segment is adjacent to at least one side of the second linear segment, and wherein the at least one side of the first linear segment is oriented at an obtuse angle with respect to the at least one side of the second linear segment.

According to one aspect of the invention, the solder reservoir portion at least partially wraps around said solder bump portion. According to another aspect of the invention, the pressure gradient creates a positive flow rate of solder to said solder bump portion during said reflow process. Furthermore, the pressure gradient can creates a negative in flow rate of solder to said solder bump portion during said reflow step. Moreover, the solder reservoir portion can include a notch to facilitate removal of said solder reservoir portion from said microelectronic substrate.

According to yet another embodiment of the invention, there is disclosed a solder bump structure on a microelectronic substrate, comprising a solder structure including a solder reservoir portion and a solder bump portion, and wherein said solder reservoir is tapered in shape.

According to one aspect of the invention, the solder reservoir portion at least partially wraps around said solder bump portion. According to another aspect of the invention, the pressure gradient creates a positive flow rate of solder to said solder bump portion during said reflow process. Furthermore, the pressure gradient can create a negative in flow rate of solder to said solder bump portion during said reflow step. Moreover, the solder reservoir portion can include a notch to facilitate removal of said solder reservoir portion from said microelectronic

substrate.

A method in accordance with the present invention for forming a solder bump structure on a microelectronic substrate comprises the steps of forming an under bump metallurgy layer on the microelectronic substrate, and forming a solder structure on the under bump metallurgy layer opposite the microelectronic substrate, wherein the solder structure includes a non-linear solder reservoir portion and a solder bump portion. The step of forming the solder structure may include the step of forming a solder structure including a plurality of solder reservoirs. In addition, the step of forming the solder structure may include the step of forming a solder bump portion and a reservoir which at least partially wraps around the solder bump portion. Yet further, the step of forming the solder structure may include the step of forming a solder structure including a solder reservoir shaped to create a pressure gradient along a length of the solder reservoir.

In accordance with another aspect of the present invention, a method of forming a solder bump structure on a microelectronic substrate comprises the steps of forming an under bump metallurgy layer on the microelectronic substrate, and forming a solder structure on the under bump metallurgy layer opposite the microelectronic substrate, wherein the solder structure included a solder bump portion and a plurality of solder reservoir portions extending therefrom.

In accordance with yet another aspect of the present invention, a method for forming a flip-chip module comprises the steps of forming a contact solder bump structure on a microelectronic substrate, forming a plurality of mechanical solder bump structures on the microelectronic substrate, wherein said mechanical solder bump structures have respective solder reservoirs associated therewith. Since the flow of molten solder from the reservoir to the bump takes time, the present invention provides a means for sequencing aspects of the soldering operation. Further , the method includes the steps of mating the microelectronic substrate to a second substrate, and reflowing the solder of the contact solder bumps and the mechanical solder bumps to bond the microelectronic substrate to the second substrate, wherein the contact solder bump becomes elongated due to the relatively larger mechanical solder bumps that will form after a brief delay.

In accordance with another aspect of the present invention, a method of forming a flip-chip module comprises the steps of forming a solder ring on a microelectronic substrate, wherein said solder ring includes at least one solder reservoir associated therewith, mating the microelectronic substrate to a second substrate in a vacuum environment to define a chamber therebetween, and reflowing the solder of the solder ring to seal the microelectronic substrate to the second substrate and to increase the volume of the chamber. Thus, because of the increased volume of the sealed chamber, the chamber is at a relatively lower pressure than the vacuum environment. The method may further include the step of forming a second solder ring substantially concentrically aligned with the solder ring, wherein the second solder ring includes at least one solder reservoir associated therewith.

Other features and advantages of the present invention will become apparent to one that is skilled in the art upon examination of the following drawings and detailed description. It is intended that all such additional features and advantages be included herein within the scope of the present invention, as defined in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1-5 are cross sectional side views of a microelectronic substrate at various stages during the manufacture of a redistribution routing conductor according to the present invention.

FIGs. 6-10 are top views of a microelectronic substrate at various stages during the manufacture of a redistribution routing conductor corresponding respectively to FIGs. 1-5.

FIGs. 11-16 are top plan views of various embodiments of controlled shaped solder reservoirs in accordance with the present invention.

FIG. 17 is a graph illustrating the relationship of the reservoir width and the internal pressure of the solder.

FIG. 18 is a cross sectional view of a flip-chip structure incorporating the solder reservoirs of the present invention.

FIG. 19 is a top plan of a substrate including mechanical contact bumps that include solder reservoirs in accordance with the present invention and electrical contact bumps.

FIGs. 20A-20C are cross sectional views of a microelectronic substrate at various stages during the manufacture of a control pressure chamber in accordance with the present invention.

FIG. 21 is a bottom plan of the top substrate in FIGs. 20A-20C.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout.

I. Redistribution Routing Conductors

A microelectronic structure **11** includes a redistribution routing conductor and a raised solder bump, as shown from the side in FIG. 5 and as shown from the top in corresponding FIG. 10. The microelectronic structure includes a contact pad **14** and passivation layer **12** on a substrate **15**. The redistribution routing conductor **17** and solder bump **21** each include respective portions of under bump metallurgy layer **16A-B** and solder layer **22A-B**.

The redistribution routing conductor **17** includes a relatively elongate solder portion **22B** (also referred to herein as a solder reservoir) on a respective elongate under bump metallurgy portion **16B**. The solder bump **21** includes an enlarged width solder portion **22A** on a respective enlarged width under bump metallurgy portion **16A**. Preferably the elongate solder portion **22B** is relatively thin while the enlarged width solder portion **22A** is raised, as shown in FIG. 5.

Accordingly, the solder bump **21** can be located at a point on the substrate relatively distant from the contact pad **14** with the redistribution routing conductor **17** providing an electrical connection therebetween. This arrangement provides the advantage that a substrate having a layout with a contact pad **14** at one predetermined location can have an associated solder bump at a second location. This can be particularly useful, for example, when a substrate has a layout with contact pads arranged for wire bonding, and it is desired to use the substrate in a flip-chip application. This solder bump and redistribution routing conductor can be fabricated simultaneously, as described below with regard to FIGs. 1-10.

While the redistribution routing conductor **17** can be straight as shown, it may also include bends and curves. Furthermore, the solder bump **21** may be circular as shown or it can have other shapes such as rectangular.

The solder bump **21** and the redistribution routing conductor **17** are preferably formed simultaneously. FIGs. 1-5 are cross-sectional side views of microelectronic structures at various stages of fabrication, while FIGs. 6-10 are corresponding top views of the same microelectronic structures. The microelectronic structure **11** initially includes a passivation layer **12** and an exposed contact pad **14** on a substrate **15**, as shown in FIGs. 1 and 6.

The substrate **15** can include a layer of a semiconducting material such as silicon, gallium arsenide, silicon carbide, diamond, or other substrate materials known to those having skill in the art. This layer of semiconducting material can in turn include one or more electronic devices such as transistors, resistors, capacitors, and/or inductors. The contact pad **14** may comprise aluminum, copper, titanium, an intermetallic including combinations of the aforementioned metals such as AlCu and $AlTi_3$, or other materials known to those having skill in the art. This contact is preferably connected to an electronic device in the substrate.

The passivation layer **12** can include polyimide, silicon dioxide, silicon nitride, or other passivation materials known to those having skill in the art. As shown, the passivation layer **12** may cover top edge portions of the contact pad **14** opposite the substrate **15**, leaving the central portion of the contact pad **14** exposed. As will be understood by those having skill in the art, the term substrate may be

defined so as to include the passivation layer **12** and contact pad **14** of FIGs. 1 and 6.

An under bump metallurgy layer **16** is formed on the passivation layer to provide a connection between the solder bump and the contact pad **14** and to provide a plating electrode, as shown in FIGs. 2 and 7. The under bump metallurgy layer **16** also protects the contact pad **14** and passivation layer **12** during subsequent processing steps, and provides a surface to which the solder will adhere. The under bump metallurgy layer preferably includes a chromium layer on the passivation layer **12** and contact pad **14**; a phased chromium/copper layer on the chromium layer; and a copper layer on the phased layer. This structure adheres to and protects the passivation layer **12** and contact pad **14**, and also provides a base for the plated solder which follows.

The under bump metallurgy layer may also include a titanium barrier layer between the substrate and the chromium layer as disclosed in U. S. Patent No. 5,767,010 entitled "Solder Bump Fabrication Methods and Structures Including a Titanium Barrier Layer," and assigned to the assignee of the present invention. This titanium barrier layer protects the passivation layer from etchants used to remove the other components of the under bump metallurgy layer and also prevents the formation of residues on the passivation layer which may lead to shorts between solder bumps and redistribution routing conductors. The titanium layer can be easily removed from the passivation layer without leaving significant residues.

Various under bump metallurgy layers are disclosed, for example, in U.S. Patent No. 4,950,623 to Dishon entitled "Method of Building Solder Bumps", U.S. Patent No. 5,162,257 to Yung entitled "Solder Bump Fabrication Method", and U.S. Patent No. 5,767,010 to Mis et al. entitled "Solder Bump Fabrication Methods and Structures Including a Titanium Barrier Layer." Each of these references is assigned to the assignee of the present invention, and the disclosure of each is hereby incorporated in its entirety herein by reference.

A solder dam **18** can be formed on the under bump metallurgy layer **16**. This solder dam **18** preferably includes a layer of a solder non-wettable material

such as titanium or chromium on the under bump metallurgy layer **16**. The solder dam **18** will be used to contain the solder if a reflow step is performed prior to removing the first (exposed) portion of the under bump metallurgy layer **16** not covered by solder, as discussed below. A mask layer **20** is then formed on the solder dam **18**. The mask layer may comprise a photoresist mask or other mask known to those having skill in the art.

The mask layer **20** is patterned to cover the solder dam over the first portion of the under bump metallurgy layer and to uncover areas of the solder dam **18** over a second portion of the under bump metallurgy layer **16** on which the solder bump and redistribution routing conductor will be formed. The uncovered portion of the solder dam is then removed thereby uncovering the second portion of under bump metallurgy layer **16**, as shown in FIGs. 3 and 8. More particularly, the second portion of the under bump metallurgy layer **16**, which is not covered by the solder dam and patterned mask layer, includes an enlarged width portion **16A** and an elongate portion **16B**.

A solder layer **22** is preferably electroplated on the second portion of the under bump metallurgy layer **16**, as shown in FIGs. 4 and 9. The solder can be electroplated by applying an electrical bias to the continuous under bump metallurgy layer **16** and immersing the microelectronic structure in a solution including lead and tin, as will be understood by those having skill in the art. This electroplating process allows solder layers to be formed simultaneously on a plurality of second portions of the under bump metallurgy layer **16**. The solder will not plate on the mask layer **20**. Alternatively, the solder can be applied by screen printing as a paste, by evaporation, by e-beam deposition, by electroless deposition or by other methods known to those having skill in the art. In addition, while lead-tin solder is used for purposes of illustration throughout the specification, other solders such as gold solder, lead-indium solder, or tin solder can be used as will be understood by those having skill in the art.

The solder layer **22** includes an elongate portion **22B** and an enlarged width portion **22A**. After removing the mask layer **20**, the microelectronic structure **11** can be heated causing the solder to flow from the elongate solder portion **22B** to

the enlarged width solder portion **22A** thereby forming a raised solder bump at the enlarged width solder portion **22A**. The solder dam **18** prevents the solder from spreading beyond the elongate **16B** and enlarged width **16A** portions of the under bump metallurgy layer **16**, as shown in FIGs. 5 and 10.

The solder will flow when heated above its liquidous temperature (approximately 299°C for solder having 90% lead and 10% tin), and this process is commonly referred to as solder reflow. During reflow, the surface tension of the solder creates a relatively low internal pressure in the enlarged width solder portion **22A** over the relatively wide geometry provided for the solder bump, and a relatively high internal pressure in the elongate solder portion **22B** over the relatively narrow geometry provided for the redistribution routing conductor.

In order to equalize this internal pressure differential, solder flows from the elongate solder portion **22B** to the enlarged width solder portion **22A**. Accordingly, the solder forms a raised solder bump at the enlarged width solder portion **22A** and a relatively thin layer of solder at the elongate solder portion **22B** over the redistribution routing conductor. When the solder is cooled below its liquidus temperature, it solidifies maintaining its shape including the raised solder bump and the thin layer of solder over the redistribution routing conductor.

It is known in the art of printed circuit board manufacture to apply solder at a uniform level on PCB lands by screen printing, and that the level of solder can be increased locally by enlarging a part of the land. *See*, Swanson, "PCB Assembly: Assembly Technology in China," *Electronic Packaging & Production*, pp. 40, 42, January 1995. To their knowledge, however, Applicants are the first to realize that solder can be electroplated on a microelectronic substrate at a uniform level and then heated to produce a raised solder bump together with a redistribution routing conductor on the substrate.

Furthermore, U. S. Patent No. 5,327,013 to Moore et al. states that a microsphere of a solder alloy can be pressed onto a pad, and that a stop formed of a polymeric solder resist material can be applied to the runner to confine the solder to the bond pad. While this patent states that the spread of solder along the runner during reflow can be limited by constricting the width of the runner section relative

to the bond pad, there is no suggestion that the relative dimensions of the runner section and the bond pad can be used to cause solder to flow from the runner to the bond pad thereby forming a multilevel solder structure. In addition, neither of these references suggest that a solder structure having an elongate portion and an enlarged width portion can be used to mask the under bump metallurgy layer in order to form a redistribution routing conductor together with a raised solder bump using only a single masking step.

The method described herein relies on differences in the surface-tension induced internal pressure of the reflowed (liquid) solder to form a thin layer of solder at the elongate solder portion **22B** and a raised solder bump at the enlarged width solder portion **22A**. The internal pressure P of a liquid drop of solder can be determined according to the formula:

$$P=2T/r,$$

where T is the surface tension of the liquid solder, and r is the radius of the drop.

Where liquid solder is on a flat wettable surface such as the under bump metallurgy layer, the formula becomes:

$$P=2T/r'.$$

In this formula, r' is the apparent radius of the liquid solder, and the apparent radius is the radius of the of the arc (radius of curvature) defined by the exposed surface of the solder. The apparent radius is dependent on the width of the underlying solder wettable layer such as the second portion of the under bump metallurgy layer which is in contact with the solder. Accordingly, the internal pressure of a reflowed solder structure is inversely proportional to the width of the second portion of the under bump metallurgy in contact with the solder. Stated in other words, a solder portion having on a relatively wide under bump metallurgy portion will have a relatively low internal pressure while a solder portion on an elongate (relative narrow) under bump metallurgy portion will have a relatively high internal pressure. The internal pressures will equalize when the apparent radii of the elongate solder portion **22B** and the enlarged width solder portion **22A** are approximately equal.

Accordingly, when the solder layer **22** with a uniform level illustrated in

FIGs. 4 and 9 is heated above its liquidus temperature, solder flows from the elongate solder portion **22B** to the enlarged width solder portion **22A** until each portion has approximately the same apparent radius thereby forming a raised solder bump. If the solder flow step is performed prior to removing the first portion of the under bump metallurgy layer **16** not covered by the solder structure, an intermetallic can be formed between the solder portions **22A-B** and under bump metallurgy portions **16A-B** adjacent the solder wherein the intermetallic is resistant to etchants commonly used to remove the under bump metallurgy. Accordingly, this intermetallic reduces undercutting of the solder during the following step of removing the first portion of the under bump metallurgy not covered by solder, as discussed in U. S. Patent No. 5,162,257 to Yung entitled "Solder Bump Fabrication Method" and assigned to the assignee of the present invention.

Preferably, the under bump metallurgy layer **16** includes a copper layer adjacent the solder structure and the solder is a lead-tin solder. Accordingly, the step of causing the solder to flow will cause the solder to react with the copper to form an intermetallic region adjacent the solder structure, and this intermetallic will comprise Cu_3Sn. This intermetallic does not readily react with etchants commonly used to remove under bump metallurgy layers thereby reducing undercutting of the solder structure.

The solder layer **22** is then preferably used as a mask to selectively etch the first portions of the solder dam **18** and under bump metallurgy **16** not covered by solder. A chemical etchant can be used which etches the under bump metallurgy layer **16** preferentially with respect to the solder portions **22A-B**. Accordingly, no additional masking step is required to pattern the under bump metallurgy layer. Stated in other words, the formation of mask layer **20** is the only masking step required to pattern the solder dam **18** (FIGs. 3 and 8), selectively expose the second portion of the under bump metallurgy layer **16** during the plating step (FIGs. 3 and 8), and remove the first portions of the under bump metallurgy layer not covered by solder after the plating step (FIGs. 5 and 10).

Alternately, the first portions of the under bump metallurgy layer **16** not covered by solder portions **22A** and **22B** can be selectively removed prior to

causing the solder to flow. In this case, the elongate **22B** and enlarged width **22A** solder portions are respectively supported on only the elongate **16B** and enlarged width **16A** under bump metallurgy portions, and while the liquid solder is wettable to the under bump metallurgy, it is not wettable to the passivation layer **12**. Accordingly, the passivation layer can contain the solder during the solder flow step, and the solder dam **18** can be eliminated.

In another alternative, the solder dam can include a solder non-wettable layer on the under bump metallurgy layer **16** and a solder wettable layer, such as copper, on the solder non-wettable layer opposite the under bump metallurgy layer, as disclosed in U. S. Patent No. 5,767,010 to Mis et al. entitled "Solder Bump Fabrication Methods and Structures Including a Titanium Barrier Layer". The solder wettable layer allows solder to be plated on portions of the solder dam as well as the second portion of the under bump metallurgy layer not covered by the solder dam or mask.

Accordingly, the mask layer **20** can uncover portions of the solder dam as well as portions of the under bump metallurgy layer **16** thereby allowing a greater volume of solder to be plated. The mask layer **20** and underlying portions of the solder wettable layer are then removed. When heat is applied to cause the solder to flow, the remaining portion of the solder wettable layer under the solder will be dissolved into the solder exposing the solder to the solder non-wettable layer. Accordingly, the solder will retreat to the second portion of the under bump metallurgy layer which is wettable.

As an example, a first portion of the under bump metallurgy layer **16** is covered by a solder dam **18** and a mask layer **20**. A second portion of the under bump metallurgy layer **16** is uncovered and has an elongate portion **16B** that is 150 micrometers wide and 500 micrometers long, and a circular enlarged width portion **16A** with a 500 micrometers diameter (or width), as shown in FIGs. 3 and 8. A uniform 35 micrometers high solder layer **22** is then electroplated on the second portion of the under bump metallurgy layer **16** including elongate portion **16A** and enlarged width portion **16B**, as shown in FIG. 4. This solder is 90% lead and 10% tin. After removing the mask layer **20**, the solder is heated above its liquidus

temperature (approximately 299°C) allowing it to flow.

The liquid solder is contained on the second portion **16A-B** of the solder wettable under bump metallurgy layer by the solder dam **18** to which the solder will not wet. Because the solder structure has varying widths, the internal pressure of the solder structure is not consistent when the height is uniform. In particular, the internal pressure of the elongate solder portion **22B** is relatively high (approximately 1.283 X 10^4 Pa or 1.86 psi) and the internal pressure of the enlarged width solder portion **22A** is relatively low (approximately 3.848 X 10^3 Pa or .558 psi) at the original solder height.

Accordingly, solder flows from the elongate solder portion **22B** to the enlarged width solder portion **22A** until the internal pressures equalize, thereby forming a raised solder bump at the enlarged width solder portion **22A**, as shown in FIGs. 5 and 10. In FIGs. 5 and 10, the solder dam **18** and the first portion of the under bump metallurgy layer **16** not covered by the solder structure have also been removed.

In this example, equilibrium is obtained at an internal pressure of approximately 3.4 X 10^3 Pa (.493 psi). At equilibrium, the elongate solder portion **22B** is approximately 10 micrometers high and the enlarged width solder portion **22A** is approximately 130 micrometers high, and both portions have a radius of curvature of approximately 281 micrometers. Accordingly, a two level solder structure can be provided with a single masking step. When cooled, this structure solidifies while maintaining its form. In addition, the elongate solder portion **22B** with a solder height of 10 micrometers is sufficient to mask the respective elongate under bump metallurgy layer portion **16B** when removing the first portion of the under bump metallurgy layer not covered by solder. The enlarged width portion of the solder structure may have a width (or diameter if the enlarged width portion is circular) of at least two times a width of the elongate portion of the solder structure in order to ensure that the solder bump formed by the method described above is sufficiently raised relative to the elongate solder portion to provide an adequate connection to a printed circuit board.

In the drawings and specification, there have been disclosed typical

preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

II. Controlled-Shaped Solder Reservoirs

As described above, the elongate solder portion **22B** functions as a solder redistribution reservoir for the enlarged with solder portion **22A**. The surface-tension induced pressure differential causes the molten solder in a relatively high pressure elongate solder portion **22B** to flow to the relatively lower pressure enlarged width portion **22A**. The increasing solder volume at the enlarged width portion **22A** forms a raised solder bump. A solder bump so formed generally has a relatively larger height than solder bumps formed without solder redistribution reservoirs when utilizing the same pad diameter and solder plating thickness. Thus, by taking advantage of the surface-tension induced pressure differential between a solder redistribution reservoir and an elongate width portion, such as a solder bump, relatively taller bumps can be advantageously achieved. The following description is of various embodiments of solder structures which take advantage of this pressure differential to produce more efficient and reliable solder structures.

With reference to FIG. 11, a solder structure **30** in accordance with the present invention as illustrated. The solder structure **30** includes a square solder redistribution reservoir **32**, and a channel **34** that connects the solder redistribution reservoir **32** to an enlarged with portion, such as bump **34**. The square solder redistribution reservoir **32** includes at least two linear segments, each having opposed sides, where at least one side of a first linear segment is oriented at an obtuse angle with respect to at least one side of a second linear segment adjacent the first linear segment. Accordingly, as a solder forming the solder structure is heated to its liquidus state to cause the solder to flow, commonly referred to as solder reflow, the solder flows from the solder redistribution reservoir **32** to the bump **36** via the channel **34** due to the internal pressure differential. The additional solder from the solder redistribution reservoir **32** increases the volume of solder

forming the solder bump, thereby forming a relatively taller solder bump. Thus, the space between adjacent bumps in an area array can be utilized to store the solder that flows into the bumps during reflow.

As an example, assume an area array flip chip with 0.125 mm diameter pads on a 0.25 mm pitch, a minimum spacing for features in the plating template of 0.025 mm, and plating solder that is 0.05mm thick. A solder bump under these circumstances would have a solder volume of 6.4 E-4 mm^3, and a height of 0.07 mm. However, by providing a solder redistribution reservoir **32** around the solder bump pad, as shown in FIG. 11, that is 0.063 mm wide and 0.25 mm square, the bump volume increases to 1.23 E-3 mm^3. Accordingly, solder bump height is significantly increased while not affecting the solder bump pitch in the array.

It is noted that the solder structure **30**, and those structures discussed below, is preferably fabricated with the single mask process described above, though it will be recognized by those of ordinary skill in the art that other suitable solid, liquid, vapor, and electromechanical deposition methods may be utilized, as well known in the art. Further, it is noted that while the solder bumps described herein are circular in shape, one having ordinary skill in the art will recognize that the solder bumps may take any geometry, such as square, rectangular or polygonal.

It is further noted that while a solder redistribution reservoir **32** is square, other geometries for the solder redistribution reservoir are within the scope of the present invention. The different geometries and dimensions of the solder redistribution reservoir may be controlled by various design parameters, such as the amount of solder to be added, the speed of flow, the minimum feature spacing, etc. For instance, as illustrated in FIG. 12, a solder structure **38** includes a U-shaped solder redistribution reservoir **40** of the same width as the solder redistribution reservoir **32** may be utilized in order to provide additional solder to the bump. As another example, a solder structure **50** comprises a bump portion **52** in a plurality of regularly extending solder redistribution reservoirs **54**, as illustrated in FIG. 13. Thus, by engineering the particular dimensions in shape of the solder redistribution reservoir, the volume, height, and area of the solder bump can be precisely controlled.

It is believed that the solder lines forming the solder redistribution reservoirs may reach a critical length where the efficiency of the solder flow begins to decreases. To improve flow at or near this critical length, and/or to better control the flow rate of the solder, a gradient line width may be utilized, as illustrated in FIGs. 14-16. As shown in FIG. 17, the line width and internal pressure are essentially inversely proportional. Thus, by designing the solder redistribution reservoir to be tapered in shape, having an increasing line width from a distal end to a proximate end adjacent the bump, the flow rate of the solder will be increased. An increase in the flow rate may be desirable with solder having a wide range of plastic flow so that the solder can be moved before it is completely molten. As illustrated in FIGs. 14 and 15, solder structures **60** and **62**, include solder redistribution reservoir **64** and **66**, respectively, which have continuous line width gradients. It is noted, however, that continuous line width gradients are not necessary for the present invention. The line width gradient may be in only a portion of the solder lines forming the solder redistribution reservoir.

Alternatively, the solder redistribution reservoir may have a line width that decreases from a distal end to a proximate end adjacent the solder bump in order to decrease the flow rate, as illustrated by the solder structure **70** having solder redistribution reservoirs **72**. Slowing the flow rate of the solder in the solder redistribution reservoirs may be desirable in various circumstances, such as with eutectic solders where rapid flow produces instabilities and unpredictability. Specifically, the instability and unpredictability with eutectic solders is caused by a variety of factors, such as not all the solder melting simultaneously, grains of higher melting point alloys, etc.

As discussed above, a small amount of solder remains in the solder redistribution reservoir after reflow. Even though the solder redistribution reservoirs described herein can be shaped and sized to take very little space on a substrate, it may still be desirable to remove the solder redistribution reservoirs after the reflow step. In accordance with the present invention, by inhibiting the complete conversion of the copper (or other wettable metal)layer of the under bump metallurgy to an intermetallic, the remaining copper may be removed in the

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under bump metallurgy etch step. The removal of the copper allows the residual solder of the solder redistribution reservoir to break off and float away in the under bump metallurgy etchant. A small area of the solder redistribution reservoir may have a narrow width or notch 74 (FIG. 16) which creates a weak point at which the solder reservoir will break off, thereby controlling the breaking point.

By way of example, one method of causing incomplete conversion of the copper in the metallurgy layer is to use a high-lead solder. Another technique involves the use of rapid solder flow, as achievable via the techniques described above, so that there is insufficient tin left in the residual solder in the solder redistribution reservoir to complete the conversion of the copper. However, it is noted that other techniques may be utilized to prevent the complete conversion of the copper, thereby creating a sacrificial copper layer that release the solder redistribution reservoir of the substrate.

Advantageously, solder bumps fabricated utilizing the solder redistribution reservoirs in accordance with the present invention are taller than solder bumps without a solder redistribution reservoir given the same pad diameter and plating thickness. This is particularly advantageous in flip chip designs where it is often difficult to adequately clean the flux and other residue from between the chip and substrate following the reflow step. The incomplete removal of flux and other residue may cause poor adhesion of the underfill epoxies, electrical leakage, or corrosion of metals. If the gap is not sufficiently large between the chip and substrate, then the boundary layer of the cleaning solution would prevent or restrict the flow of the cleaning solution between the chip and substrate.

However, the taller solder bump resulting from the use of the solder redistribution reservoirs will improve the effectiveness of the cleaning solution by increasing the gap between the chip substrate.

The underfill process will likewise benefit from the increased gap size. The underfill epoxy is typically of low viscosity and may not flow between the chip and substrate if the gap is too small. The taller solder bumps provide improved clearance, thereby resulting in better underfill. The structure shown in FIG. 11, when scaled to a pitch of 0.250 mm and plated to a height of 0.050 mm, could be

expected to increase the gap from 0.07 mm to 0.100 mm.

Furthermore, the taller the solder bump, the more mechanically reliable the solder bump. This is primarily due to the reduction and strain per unit length discussed above. Of special benefit is the reduction of the strain per unit length to below the elastic limit for the solder. This will eliminate the plastic damage which is the cause of solder fatigue failure.

An advantageous application of the present invention is illustrated in FIGs. 18 and 19, whereby the reliability of electrical connections in a flip chip device are improved. In particular, with reference to FIG. 18, a chip **80** may comprise mechanical bumps **82** which have one or more solder reflow reservoirs **84** in accordance with the present invention associated therewith, and one or more contact solder bump **86** for forming electrical contacts between the chip **80** and a substrate **88** (FIG. 19). Given substantially uniform plating thickness across chip **80**, the mechanical bumps **82** will have a greater volume that the contact bumps **86**, and therefore, will be taller. It has been determined that the contact bumps **86** should have a contact pad **90** as equal to or larger than the contact pads **92** associated with the mechanical bumps **82**. By using contact pads of the same size or larger with the contact bumps **86**, the mechanical bumps **82** will not grow larger that the contact bumps **86** until the contact bumps **86** have soldered to the substrate **88**. Alternatively, the flow rate of the soldered to the mechanical bumps **86** from the solder redistribution reservoir may be slowed using a solder redistribution reservoir of a suitable dimension and shape, as described above. As shown in FIG. 19, the taller mechanical bumps **82** create a larger gap or opening between the chip **80** and substrate **88**, which stretches the contact bumps **86**. As discussed above, the elongated contact bumps **86** are more reliable because the strain per unit length is reduced. It is noted that the bump designs and configurations of FIGs. 18 and 19 are merely exemplary of a bump and associated solder redistribution reservoir which can be utilized to stretch or elongate a contact bump to improve the reliability of the contact bump.

In yet another advantageous application of the present invention, an improved vacuum may be formed in a sealed chamber, as illustrated in FIGs. 20A-

20C, and 21. In particular, a lid or cap **102** is patterned with a soldered seal ring **104** for bonding with a substrate **106** for creating a sealed chamber **108**. In the embodiment illustrated, a second seal ring **110** is provided for redundancy and improved reliability, though it is not necessary for the present invention, as best illustrated in FIG. 21. Nonetheless, the second seal ring **110** reduces the pressure differential across the first seal ring **104**. Associated with each seal ring **104, 110** is at least one solder redistribution reservoir **111** in accordance with the present invention. While the solder redistribution reservoirs **112** are rectangular in the illustrative embodiment, it is recognized that the solder redistribution reservoirs can be shaped and sized as described herein to achieve a desired result.

A microelectromechanical system (MEMS) device **112**, or other device favoring a vacuum environment, is disposed inside the chamber **108**. While the MEMS device **112** is shown fabricated on the substrate **106**, it will be recognized by those of ordinary skill in the art that the MEMS device can be fabricated on either or both the lid **102** and the substrate **106**.

On the substrate, bonding regions **114** are provided in the form of a metallization or other conventional solder wettable material for bonding to the respective solders seal rings **104, 110**. The fabrication of the bonding regions is well known and need not be described further herein. Alternatively, solder dams may be utilized, as with cap **102**. It is noted that the solder seal rings **104, 110** may be square as shown, or alternatively, circular, rectangular, polygonal, or any other shape.

With particular reference to FIGs. 20A-20C, the cap **102** is initially plated with solder seal rings **104, 110**. The cap **102** is then placed on the substrate **106** so that the solder ring aligns with the solder wettable pads on the substrate **106**. This procedure is preferably performed in a vacuum environment so that the resulting chamber **108** is at the pressure of the vacuum environment. Upon reflow, the solder seal rings **104, 110** increase in size with the additional solder from the solder redistribution reservoirs, thereby expanding the volume of the chamber **108**. The increase in volume decreases the pressure in the chamber **108**. Thus, the pressure in the chamber **108** will be less than that of the vacuum environment in which it

was sealed.

As an example, using the increase in gap height given above, the gap volume will increase from 0.070mm*A, where A is the area enclosed by the seal ring, to 0.1mm*A. The volume increase is then 10/7 or 1.43 times greater. Since pressure is inversely proportional to volume, the pressure will be 30% lower than without the increased gap.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention, and although specific terms are employed, they are used in a generic and descriptive sense only, and not for the purposes of limitation; the scope of the invention being set forth in the following claims.

CLAIMS

Wherefore, the following is claimed:

1. A solder bump structure on a microelectronic substrate, comprising a solder structure including a solder reservoir portion and a solder bump portion, and wherein said solder reservoir portion is non-linear and shaped to create a pressure gradient along a length of said solder reservoir portion during a solder reflow process wherein said solder reservoir portion includes a first linear portion and a second linear portion, each having at least one straight side, and wherein a straight side of said first linear portion forms an obtuse angle with respect to a straight side of said second linear portion.

2. A microelectromechanical system (MEMS) module, comprising:

a substrate and a lid in spaced apart relationship;

a solder ring which bonds said lid to said substrate to define a sealed chamber therebetween, wherein said solder ring includes at least one solder reservoir associated therewith; and

a MEMS device formed in said chamber.

3. The MEMS module of Claim 2, further including a second solder ring substantially concentrically aligned with said solder ring, and wherein said second solder ring includes at least one solder reservoir associated therewith.

4. The MEMS module of Claim 2, further comprising elongated electrical contacts in said chamber, wherein said elongated electrical contacts electrically connect said lid to said substrate.

5. The MEMS module of Claim 2, wherein said chamber includes a controlled environment maintained at a vacuum.

6. A method of forming a solder bump structure on a microelectronic substrate including a layer of a semiconducting material, comprising the steps of:

forming an under bump metallurgy layer on the microelectronic substrate including the layer of the semiconducting material; and

forming a solder structure on the under bump metallurgy layer opposite the microelectronic substrate including the layer of the semiconducting material, the solder structure including a solder bump portion and a plurality of solder reservoir portions extending therefrom.

7. A method of forming a flip-chip module, comprising the steps of:

forming a solder ring on a microelectronic substrate, wherein said solder ring includes at least one solder reservoir associated therewith;

mating the microelectronic substrate to a second substrate in a vacuum environment to define a chamber therebetween; and

reflowing the solder of the solder ring to seal the microelectronic substrate to the second substrate so as to increase the volume of the chamber, whereby the chamber is at a relatively lower pressure than said vacuum environment.

8. The method of Claim 7, further including the step of forming a second solder ring substantially concentrically aligned with said solder ring, wherein said second solder ring includes at least one solder reservoir associated therewith.

9. A solder bump structure on a microelectronic substrate, comprising a layer of a semiconducting material and a solder structure including a solder reservoir portion and a solder bump portion, and wherein said solder reservoir portion comprises:

a first linear segment on the microelectronic substrate comprising the layer of the semiconducting material, wherein the first linear segment has opposed sides, and

a second linear segment on the microelectronic substrate comprising the layer of the semiconducting material, wherein the second linear segment has opposed sides,

wherein at least one side of the first linear segment is adjacent to at least one side of the second linear segment, and wherein the at least one side of the first linear segment is oriented at an obtuse angle with respect to the at least one side of the second linear segment.

10. The solder bump structure of Claim 9, wherein said solder reservoir portion at least partially wraps around said solder bump portion.

11. The solder bump structure of Claim 9, wherein a pressure gradient creates an increased flow rate of solder to said solder bump portion during said reflow process.

12. The solder bump structure of Claim 9, wherein a pressure gradient creates a decreased flow rate of solder to said solder bump portion during said reflow step.

13. The solder bump structure of Claim 9, wherein said solder reservoir portion includes a notch to facilitate removal of said solder reservoir portion from said microelectronic substrate.

14. A solder bump structure on a microelectronic substrate, comprising a solder structure including a solder reservoir portion and a solder bump portion, and wherein said solder reservoir is tapered in shape.

15. The solder bump structure of Claim 14, wherein said solder reservoir portion at least partially wraps around said solder bump portion.

16. The solder bump structure of Claim 14, wherein a pressure gradient creates an increased flow rate of solder to said solder bump portion during said reflow process.

17. The solder bump structure of Claim 14, wherein a pressure gradient creates a decreased flow rate of solder to said solder bump portion during said reflow step.

18. The solder bump structure of Claim 14, wherein said solder reservoir portion includes a notch to facilitate removal of said solder reservoir portion from said microelectronic substrate.