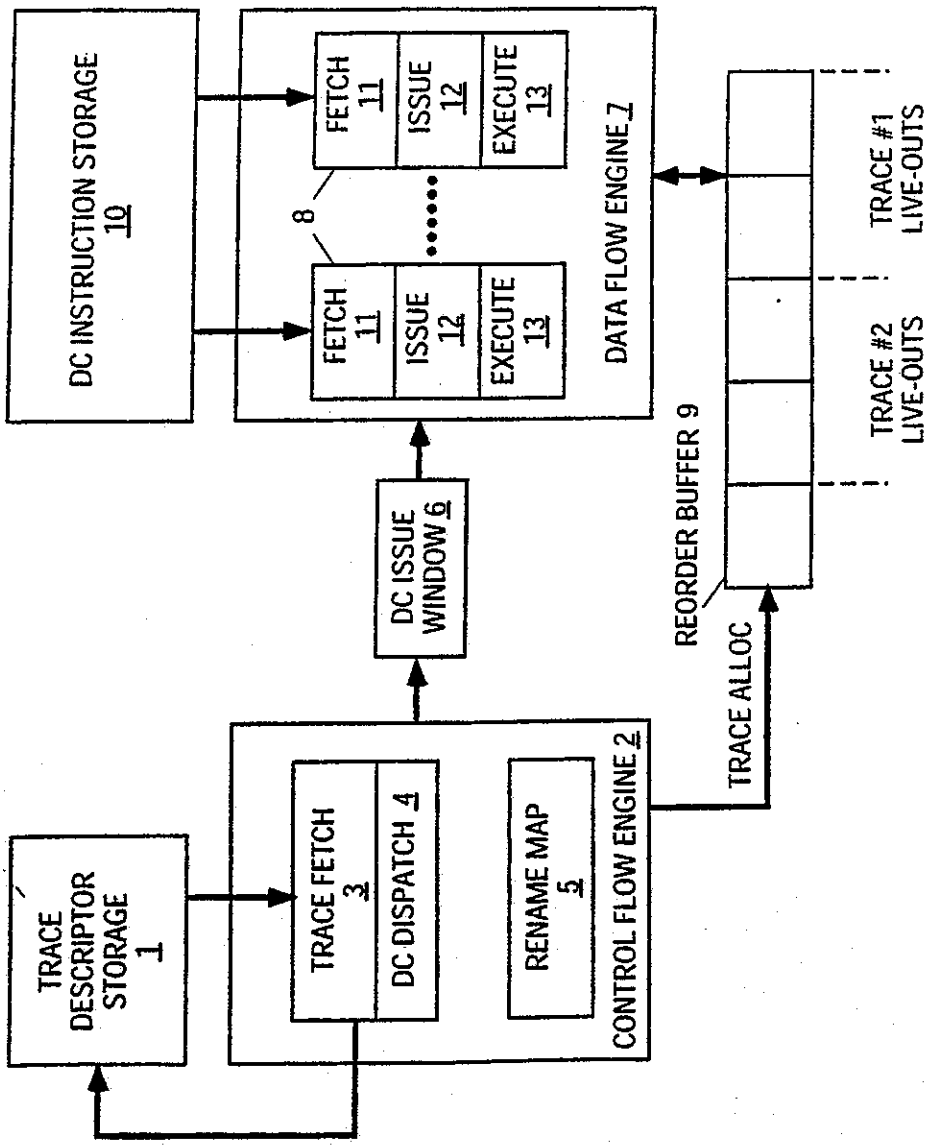

DC INSTRUCTION STORAGE 10
FETCH 11
ISSUE 12
EXECUTE 13
8
FETCH 11
ISSUE 12
EXECUTE 13
DATA FLOW ENGINE 7
TRACE #1 LIVE-OUTS
TRACE #2 LIVE-OUTS
REORDER BUFFER 9
DC ISSUE WINDOW 6
TRACE DESCRIPTOR STORAGE 1
TRACE FETCH 3
DC DISPATCH 4
RENAME MAP 5
CONTROL FLOW ENGINE 2
TRACE ALLOC

FIG. 1

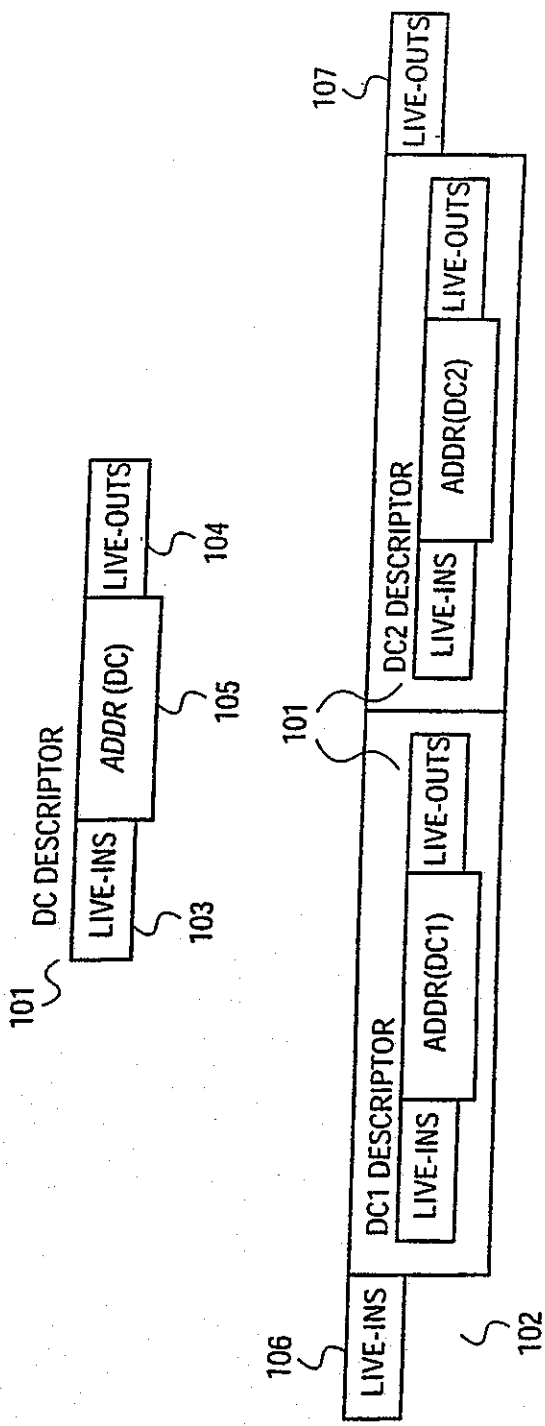

DC DESCRIPTOR
LIVE-INS
ADDR (DC)
LIVE-OUTS
101
103
105
104
DC1 DESCRIPTOR
LIVE-INS
ADDR(DC1)
LIVE-OUTS
DC2 DESCRIPTOR
LIVE-INS
ADDR(DC2)
LIVE-OUTS
101
107
106
102

FIG. 2

Trace

```
i00,  aw      r3, 0(r6)
i01,  addiu   r6, r6, 4
i02,  addiu   r7, r7, 1
i03,  alti    r2, r7, 32
i04,  bne     r2, r0, 0x42b3a8
i05,  lw      r5, 0(r6)
i06,  addu    r3, r0, r0
i07,  altu    r2, r5, r4
i08,  bne     r2, r0, 0x42b3d0
i09,  sw      r3, 0(r6)
i10,  addiu   r6, r6, 4
i11,  addiu   r7, r7, 1
i12,  slti    r2, r7, 32
i13,  bne     r2, r0, 0x42b3a8
```

FIG. 3

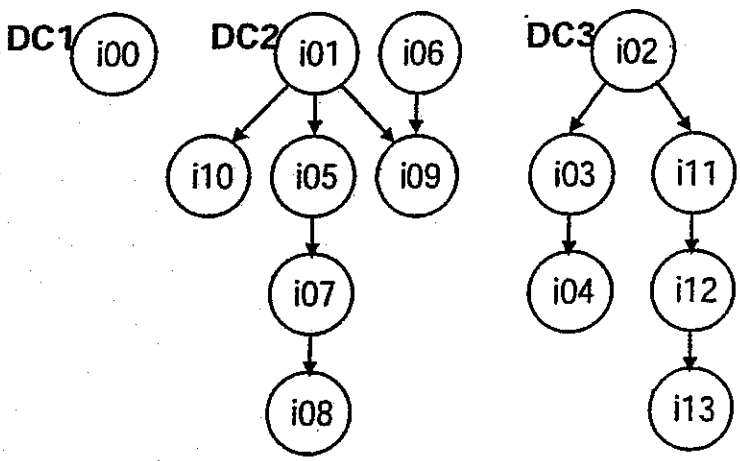


FIG. 4

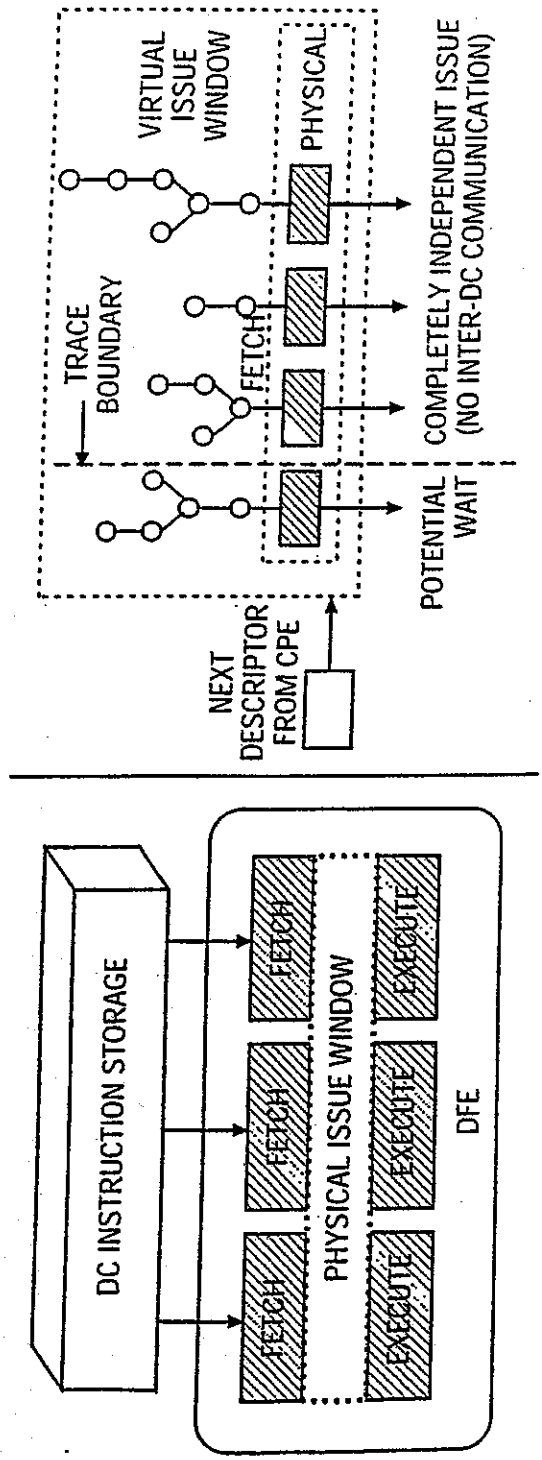

DC INSTRUCTION STORAGE
FETCH
FETCH
FETCH
PHYSICAL ISSUE WINDOW
EXECUTE
EXECUTE
EXECUTE
DFE
NEXT DESCRIPTOR FROM CPE
TRACE BOUNDARY
VIRTUAL ISSUE WINDOW
PHYSICAL
FETCH
POTENTIAL WAIT
COMPLETELY INDEPENDENT ISSUE (NO INTER-DC COMMUNICATION)

FIG. 5

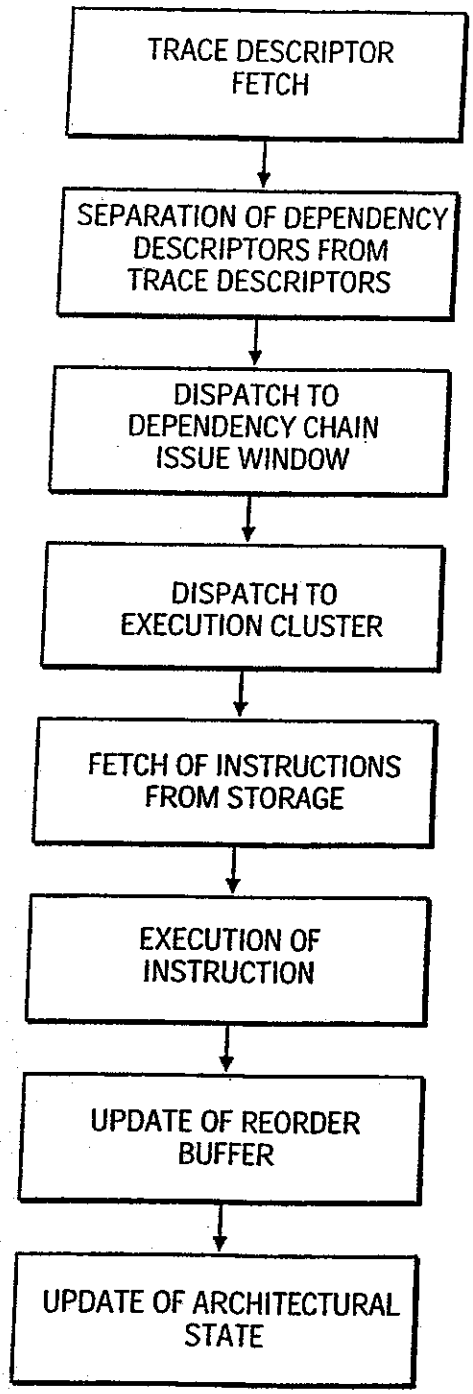

TRACE DESCRIPTOR FETCH
SEPARATION OF DEPENDENCY DESCRIPTORS FROM TRACE DESCRIPTORS
DISPATCH TO DEPENDENCY CHAIN ISSUE WINDOW
DISPATCH TO EXECUTION CLUSTER
FETCH OF INSTRUCTIONS FROM STORAGE
EXECUTION OF INSTRUCTION
UPDATE OF REORDER BUFFER
UPDATE OF ARCHITECTURAL STATE

FIG. 6

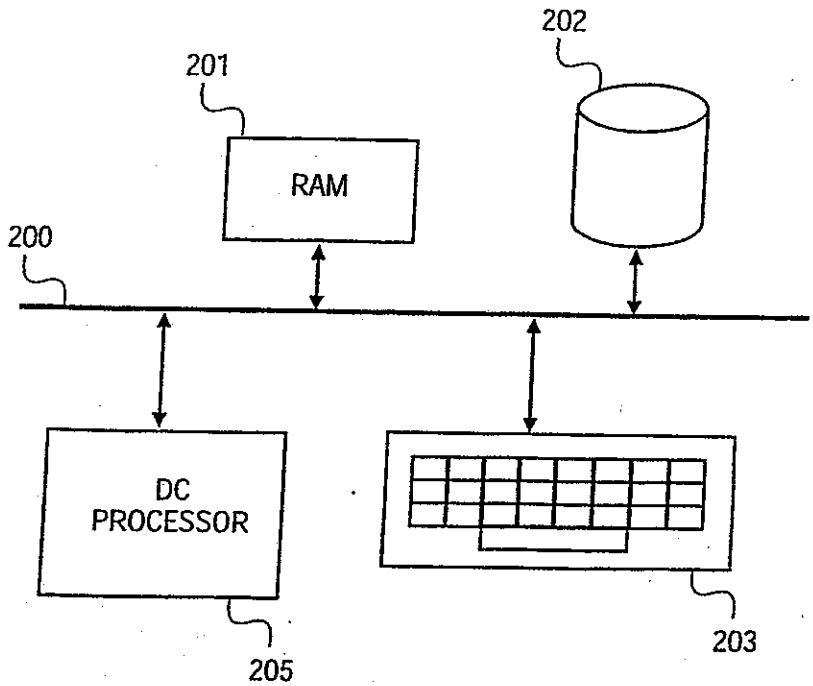


FIG. 7