

LEADED MCM PACKAGE AND METHOD THEREFOR

This invention relates generally to the field of semiconductor device manufacture and more particularly to the packaging of semiconductor devices with integrated circuit chips to be used in an electronic assembly, such as a printed circuit board.

In the electronics industry, the quest for smaller electronic devices which perform better at a lower cost is ongoing. This is especially true of the portable electronics and wireless communications sector which has undergone recent rapid growth. In particular, there is often a need for a single semiconductor package which can perform a variety of diverse functions with high performance.

Generally speaking, two different technologies which are able to provide complete electronic systems in a single package may be identified. The first technology is known as system-on-a-chip (SoC). This technology involves integrating several integrated circuits having different functions (such as memory, logic, analog etc) into a single composite chip at the die level. The resultant single chip is generally smaller in size than the combined size of individual component integrated circuits. Further, the system performance is generally superior due to the shorter electrical paths and lower electrical parasitics between the component integrated circuits.

The second technology is known as system-in-a-package (SiP) which involves packaging several discrete integrated circuit chips in a single package. In common with SoC, the main objective of SiP is to minimize the required form factor of the IC components on the systems board while increasing the systems functionality and performance.

In recent times, SiP has become increasingly popular compared to the SoC solution because it benefits from a number of additional advantages. In particular, SiP packages are easier to produce than SoC chips and usually they are more cost effective and have a shorter time-to-market.

The SiP technology can be further broken down into two sub-types of MCM (multi-chip module) or MCP (multi-chip package). The distinction between MCM

and MCP lies mainly in the type of substrate used and the number of IC components in the total package. A MCM generally has larger substrates with higher densities of various materials (ceramic, thin-film, laminate) and uses different types of die attachment methods (flip chip, TAB, wire bond) within the same package. In contrast, a MCP uses a cheaper substrate material (usually laminates) and has a fewer number of component dies (about 2-3). Interconnects are usually made by wire bonding but flip chip interconnect is also possible. Furthermore, the pin count of MCPs is usually lower than the pin count of MCMs.

The substrates used in MCPs and MCMs are generally ball grid arrays (BGAs) or land grid rays (LGAs). It would, however, be desirable to have leaded MCM/MCPs so that manufactures who want to adopt SiP for their semiconductor devices can comply with leaded packaging formats. A leaded package offers much better solder joint fatigue reliability compared to a leadless package such as LGA or BGA. In particular, the leads of the leaded package provide for more solder attachment compliance to accommodate expansion mis-match between the package and the board during thermal cycling. For leadless packages such as LGA, the attachment compliance is much lower, resulting in a poorer soldered joint fatigue reliability.

The present invention relates to a novel semiconductor package using SiP technology with leads. Further, the present invention relates to a method of packaging a leaded multi-chip package.

Accordingly, the present invention provides a method of packaging a semiconductor device, said method comprising:

- attaching a plurality of integrated circuit chips to first side of a substrate;
- attaching a bond wire between a bond pad on one of said plurality of integrated chips and a first connection on said first side of said substrate;
- encapsulating said plurality of integrated circuit chips and said bond wire in a moulding compound;
- attaching a metallic leadframe to a second side of said substrate;

electrically connecting said metallic leadframe to a second connection on said second side of said substrate so as to provide an electrical pathway between said one of said plurality of integrated chips and said metallic leadframe;

encapsulating at least the electrical connection which connects the metallic
5 leadframe to said second connection in a moulding compound.

The invention enables multiple integrated circuit chips (possibly having different functions) to be packaged in leaded packages, using a combination of substrate and leadframe. A leadframe die paddle is not required in a device manufactured according to the present invention. The invention therefore represents
10 a feasible option for manufacturers who would like to adopt system-in-package technology using leaded packages. The invention provides a compact and easy to manufacture package available at low cost. Furthermore, the present invention also enables manufacturers to advance to a system-in-package platform for their devices without having to make major changes to their existing test and surface mount
15 assembly infrastructure. This is because the method of the present invention uses a combination of different techniques readily achievable with conventional and widespread technology.

Preferably, the method also comprises printing at least one conductive trace on the substrate before the step of attaching a plurality of integrated circuit chips. In
20 this case, the conductive trace may further be covered with a layer of soldermask material which has portions selectively removed to reveal portions of the printed conductive trace. These extra steps may be carried out on either side of the substrate. The conductive traces thus revealed are useful for electrically connecting the integrated circuit chips or leadframe to the substrate. Advantageously, a plurality of
25 such conductive traces and corresponding holes in the soldermask material are used.

Preferably, a plurality of bond wires are attached between the bond pads on the integrated chips and the bond fingers (connectors) on the first side of the substrate. All of these wires are preferably encapsulated in the moulding compound so as to electrically isolate the first side of the substrate from the environment.

30 The metallic leadframe is preferably attached to the perimeter of the second side of the substrate so that, when viewed in plan view, part of the metallic leadframe

overlaps the substrate and another part projects outwardly from it. The metallic leadframe is preferably attached to the conductive traces on the second side of the substrate using an adhesive tape. Further, the metallic leadframe may be connected to the second bond fingers (connectors) on the second side of the substrate using
5 either a bonding wire or anisotropic adhesive. Advantageously, a number of electrical connections are made between respective parts of the metallic leadframe and one of a plurality of second bond fingers. In such cases, it is preferable that the various parts of the metallic leadframe are electrically isolated from one another so that each second bond finger is connected to an isolated part of the metallic
10 leadframe.

The step of encapsulating at least the electrical connection preferably comprises also encapsulating the part of the metallic leadframe connected to the electrical connection and the whole of the second bond finger. The moulding compound used in the encapsulation may have an area when viewed perpendicularly
15 to the substrate which is smaller than the area of the second side of the substrate. Alternatively, it can have an area larger than the area of the second side of the substrate. This second feature is preferably obtained by encapsulating the entire semiconductor device in moulding compound. In this case, only those parts of the metallic leadframe which are remote from the parts of the metallic leadframe
20 attached to the substrate are visible or accessible. All the other components are completely encased in moulding compound.

Preferably, the parts of the metallic leadframe which are visible after moulding are bent or otherwise formed into various shapes, such as a gull-wing shape or a J-shape.

25 The present invention also provides a semiconductor package comprising:
a substrate;
a plurality of integrated circuit chips attached to a first side of said substrate;
a bond pad on one of said plurality of integrated circuit chips;
a first connector on said first side of said substrate;
30 at least one bond wire connecting said bond pad to said first connector;

first moulding compound which encapsulates said plurality of integrated circuit chips and said at least one bond wire;

a metallic leadframe attached to a second side of said substrate;

a second connector on said second side of said substrate, said second
5 connector being in electrical connection with said first connector;

at least one electrical connection which electrically connects said metallic leadframe to said second connector;

second moulding compound which encapsulates said at least one electrical connection.

10 The substrate is preferably formed of a plurality of layers which are laminated together. Further, the substrate preferably comprises printed conductive traces on one or both sides and a layer of soldermask on top of these traces. Portions of the soldermask may then be removed so as to reveal portions of the printed conductive traces underneath.

15 The metallic leadframe and integrated chips are preferably attached to islands of soldermask on opposite sides of the substrate.

A layer of adhesive tape is preferably present to adhere the substrate to the metallic leadframe.

Preferably the metallic leadframe has portions which are gull-wing shaped or
20 J-shaped.

The present invention also encompasses a printed circuit board or electronic device which comprises a semiconductor package as claimed or a semiconductor package manufactured according to the claimed method.

The present invention will now be described by way of non-limitative
25 example only, with reference to the accompanying drawings, in which:-

Figures 1-6 show various steps in a method of packaging a semiconductor device according to the present invention which are common to all four embodiments of the present invention;

Figures 7 and 8 show the final steps in a method of packaging a
30 semiconductor device in accordance with the first embodiment of the present invention;

Figures 7 and 9 show the final steps in a method of packaging a semiconductor device in accordance with the second embodiment of the present invention;

Figures 10 and 11 show the final steps in the method of packaging a semiconductor device in accordance with the third embodiment of the present invention;

Figures 10 and 12 show the final steps in the method of packaging a semiconductor device in accordance with the fourth embodiment of the present invention.

Detailed embodiments of the invention will now be described.

Figures 1-6 schematically illustrate method steps common to all embodiments and these will now be described.

Figure 1 shows a laminated substrate (1) which has printed conductive traces (2) on both sides. The conductive traces are not shown in the Figures but it is to be understood that they are a very thin layer on the surface of the substrate. The conductive traces are in turn covered with a layer of soldermask material which has had some designated areas removed so as to reveal the metallic conductive traces and leave islands (3) of soldermask material on the substrate. The conductive traces on the top side (first side) of the substrate (1) comprise a plurality of bond fingers (15). These bond fingers (15) are an integral part of the conductive traces. Similarly, the conductive traces on the second side of the substrate comprise bond fingers (16). The conductive traces on each side of the substrate (1) are connected together by conductive vias that connect the traces on the top side to the corresponding traces on the bottom side of the substrate (1)

As is shown in Figure 2, a plurality of integrated circuit chips (4) are attached to the islands of soldermask material (3) on the substrate. These integrated circuit chips (4) may perform substantially any function, such as memory, logic, analog electronics etc.

Figure 3 shows the next step in the process in which bonding wires (5) are connected at one end to bond pads on the integrated circuit chips and at the other end

to the bond fingers (15) on the conductive traces on the substrate (1). This procedure serves to electrically connect the integrated circuit chips to the substrate.

The first side of the substrate (1) which has on it the integrated circuit chips (4) and the bonding wires (5) is then encapsulated with a moulding compound (6) so as to isolate the integrated circuit chips (4) and bonding wires (5) from the outside environment.

In the next step shown in Figure 5, a metallic leadframe (7) is attached to the second (bottom) surface of the substrate (1). In particular, it is attached to one of the islands of soldermask (3) in this case by use of an adhesive tape (8). However, any suitable adhesive mixture/device may be used. The purpose of the leadframe (7) is to provide external electrical contacts for the whole package so that electrical signals may be routed to and from the integrated circuit chips (4) on the first side of the substrate (1).

The metallic leadframe (7) is then electrically connected to the conductive traces on the second side of the substrate by bonding wire (9) (see Figure 6). Again, bond fingers (16) on the conductive traces are used to connect the bonding wire to the conductive trace. Alternatively, anisotropic conductive adhesive may be used to connect the leadframe (7) to the conductive traces on the second side of the substrate in which case the bond fingers (16) are not required. The anisotropic adhesive conducts only in the vertical direction after attachment. It comprises many fine conductive fillers uniformly distributed in a resin binder, which is usually epoxy based. The conductivity is provided by the fine conductive particles (usually spherical) which interlink when the adhesive is compressed vertically. There is no electrical conduction in the lateral direction. The resin binder is compressed in the vertical direction while it sets so as to provide a vertical conduction path. After the resin has cured, this connection becomes permanent and the pressure can be removed. The leadframe comprises a number of electrically isolated separate portions (not shown) so that each bond finger on a lower side of the substrate is connected to a separate part of the leadframe (7).

First and Second Embodiments

Figures 7-9 show first and second embodiments of the present invention.

In Figure 7 (common to both embodiments), moulding compound has been
5 used to encapsulate the bonding wires on the second side of the substrate and part of
the leadframe. The encapsulation is such that the outline of the mould is smaller than
both the outline of the substrate when viewed perpendicularly and the outline of the
encapsulation on the first side of the substrate. This fact facilitates the moulding
process. However, the leadframe that is used must be pre-plated if chemical attack to
10 the laminate edges is to be avoided.

Figure 8 shows the first embodiment where the leadframe (7) is bent so as to
be formed into the shape of a gull-wing (11).

Figure 9 shows the second embodiment similar to the first embodiment
except that the leadframe (7) has been shaped into a J-shape (12).
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Third and Fourth Embodiments

Figures 10-12 show third and fourth embodiments of the present invention.

20 In these cases, the entire package shown in Figure 6 is encapsulated in
moulding compound. Only the portions of the leadframe remote from the portions
where the leadframe is attached to the substrate are revealed. This has the advantage
that the edges of the laminate substrate are protected by the moulding compound and
so pre-plating is unnecessary. The drawback is that the package is slightly bigger as
25 a whole.

Figure 11 shows the third embodiment of the invention in which the entire
structure is totally encapsulated and the leadframe (7) is bent into a gull-wing shape
(13).

Figure 12 shows the fourth embodiment of the invention, similar to Figure
30 11, except that the leadframe (7) is now bent into a J-shape (14).

The above methods may be carried out using components manufactured of materials standard in the art. Preferably, however, the following materials are used for the various components:

5	Component	Material
	Substrate	Bismaleimide Triazine resin or FR4
	Conductive Traces	Copper with Nickel/Gold finish
	Soldermask Material	Photo-imageable dielectric resist (for example Taiyo PSR 4000)
	Bonding Wires	Gold
10	Moulding Compound	Epoxy resin based with silica fillers
	Adhesive Tape	Epoxy based
	Anisotropic conductive adhesive	Non conductive epoxy resin with fine conductive fillers

CLAIMS

1. A method of packaging a semiconductor device, said method comprising:
 - 5 attaching a plurality of integrated circuit chips to first side of a substrate;
attaching a bond wire between a bond pad on one of said plurality of
integrated chips and a first connection on said first side of said substrate;
encapsulating said plurality of integrated circuit chips and said bond wire in a
moulding compound;
 - 10 attaching a metallic leadframe to a second side of said substrate;
electrically connecting said metallic leadframe to a second connection on said
second side of said substrate so as to provide an electrical pathway between said one
of said plurality of integrated chips and said metallic leadframe;
encapsulating at least the electrical connection which connects the metallic
15 leadframe to said second connection in a moulding compound.
2. A method according to claim 1 further comprising printing at least
one conductive trace on said substrate before said step of attaching a plurality of
integrated circuit chips.
- 20 3. A method according to claim 2, further comprising covering said at
least one conductive trace with a layer of soldermask material and selectively
removing parts of said soldermask material to reveal portions of said printed
conductive trace before said step of attaching a plurality of integrated circuit chips.
- 25 4. A method according to claim 2 or 3 wherein a plurality of conductive
traces are printed.
5. A method according to any one of the proceeding claims, wherein a
30 plurality of bond wires are attached between respective bond pads on said plurality of
integrated chips and a plurality of connections on said first side of said substrate.



6. A method according to claim 5, wherein said plurality of bond wires are encapsulated in a moulding compound.

7. A method according to any one of the preceding claims, wherein said
5 metallic leadframe is attached to the perimeter of said second side of said substrate.

8. A method according to any one of the preceding claims, wherein said metallic leadframe is attached to said second side of said substrate using an adhesive tape.

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9. A method according to any one of the preceding claims, wherein said metallic leadframe is electrically connected to said second connection using a bonding wire.

15 10. A method according to any one of the preceding claims, wherein said metallic leadframe is electrically connected to said second connection using an anisotropic conductive adhesive.

11. A method according to any one of the preceding claims, wherein a
20 plurality of electrical connections are made between respective parts of said metallic leadframe and one of a plurality of second connections on said second side of said substrate.

12. A method according to claim 11, wherein said parts of said metallic
25 leadframe are electrically isolated from one another

13. A method according to any one of the preceding claims, wherein said step of encapsulating at least the electrical connection comprises encapsulating with moulding compound the electrical connection and the part of the metallic leadframe
30 and second connection connected thereto so as to create a continuous area of



moulding compound on said second side of said substrate, said continuous area being smaller than the area of the second side of said substrate.

14. A method according to any one of claims 1 to 12, wherein said step of
5 encapsulating at least the electrical connection comprises encapsulating the entire device with moulding compound so as to only reveal those parts of the metallic leadframe which are remote from the parts of the metallic leadframe which are attached to the second side of solid substrate.

10 15. A method according to any one of the preceding claims, further comprising bending or otherwise forming those parts of the metallic leadframe which are remote from the parts of the metallic leadframe which are attached to the second side of said substrate into a predetermined shape.

15 16. A method according to claim 15, wherein said predetermined shape is a gull-wing shape or a J-shape.

17. A semiconductor package comprising:
a substrate;
20 a plurality of integrated circuit chips attached to a first side of said substrate,
a bond pad on one of said plurality of integrated circuit chips;
a first connector on said first side of said substrate;
at least one bond wire connecting said bond pad to said first connector;
first moulding compound which encapsulates said plurality of integrated
25 circuit chips and said at least one bond wire;
a metallic leadframe attached to a second side of said substrate;
a second connector on said second side of said substrate, said second
connector being in electrical connection with said first connector;
at least one electrical connection which electrically connects said metallic
30 leadframe to said second connector;



second moulding compound which encapsulates said at least one electrical connection.

18. A semiconductor package according to claim 17, wherein said
5 substrate is formed of a plurality of layers laminated together.

19. A semiconductor package according to claim 17 or 18, further comprising printed conductive traces on both sides of said substrate.

10 20. A semiconductor package according to claim 19, wherein said electrical connection connects said metallic leadframe to a conductive trace printed on the second side of said substrate.

21. A semiconductor package according to claim 19 or 20, further
15 comprising a layer of soldermask material covering said conductive traces except in portions where the soldermask material has been selectively removed to reveal portions of the printed conductive traces.

22. A semiconductor package according to claim 21, wherein said
20 plurality of integrated chips are each attached to separate islands of soldermask material on the first side of said substrate.

23. A semiconductor package according to any one of claims 17 to 22,
further comprising a layer of adhesive tape between said substrate and said metallic
25 leadframe.

24. A semiconductor package according to any one of claims 17 to 23,
wherein said second moulding compound has an area parallel to the substrate which is smaller than the area of the second side of said substrate.



25. A semiconductor package according to any one of claims 17 to 23, wherein said first and second moulding compounds have areas parallel to the substrate which are substantially the same and which are each larger than the area of either the first or second sides of the substrate.

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26. A semiconductor package according to any one of claims 17 to 25, wherein said metallic leadframe has external portions which are gull-wing shaped or J-shaped.

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27. A printed circuit board comprising a semiconductor package according to any one of claims 17 to 26 or a semiconductor device packaged according to the method of any one of claims 1 to 16.

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28. An electronic device comprising a semiconductor package according to any one of claims 17 to 26 or a semiconductor device packaged according to the method of any one of claims 1 to 16.

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29. A method of packaging a semiconductor substantially as hereinbefore described with reference to Figures 1 to 12 of the accompanying drawings.

30. A semiconductor package constructed and arranged substantially as hereinbefore described with reference to Figures 1 to 12 of the accompanying drawings.

