

DESCRIPTION**TITLE: SUBSTRATE COMPRISING A THICK BURIED DIELECTRIC LAYER
AND METHOD FOR PREPARING SUCH A SUBSTRATE**

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FIELD OF THE INVENTION

The present invention relates to a substrate of the semiconductor-on-insulator type, comprising a charge trapping layer, the insulating (or dielectric) layer having a relatively high thickness of greater than 200 nm. These substrates are applicable notably in the field of radiofrequency integrated devices, which is to say electronic devices that process signals in the frequency range between about 3 kHz and 300 GHz, for example in the field of telecommunications (telephony, Wi-Fi, Bluetooth, etc.). These substrates are also applicable in particular in the field of photonics. The invention also relates to a method for manufacturing such a substrate.

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TECHNOLOGICAL BACKGROUND OF THE INVENTION

Document WO2022023630 discloses that the formation of a final substrate of the semiconductor-on-insulator type comprising a charge trapping layer and a thick dielectric layer (more than 200 nm thick, according to this document) is particularly complicated. According to the introduction of this document, it is preferable in industry to place this dielectric layer on the support substrate of the final substrate, and the dielectric layer, made of silicon oxide, can be obtained by oxidation of a surface portion of the

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electric-charge trapping layer. The oxidation step tends to make the support substrate deform and to result in a significant curvature (denoted by the term "bow" in the terminology used in the field of semiconductors which is defined as the deviation of a centre point of the median surface of the substrate from a reference plane). This bow is generally measured by interferometry, for example using a WaferSight™ instrument from KLA. The presence of such a bow complicates the step of transferring the upper layer of the substrate, and more generally the handling of the support substrate on the production line by conventional equipment. It is generally sought to limit this bow to less than 60 micrometres, or preferably to less than 40 micrometres, for a disc-shaped substrate having a diameter of 300 mm.

Furthermore, it is essential in numerous applications that the exposed surface of the upper layer is very smooth and exhibits a roughness much less than 0.5 nm measured in root mean square terms over a field of atomic force measurement of 30 micrometres by 30 micrometres. To obtain an upper layer exhibiting such a roughness, it is known to subject the substrate to one or more thermal anneals in a neutral or reducing atmosphere after the upper layer has been transferred to the support substrate.

This anneal can be what is referred to as a "rapid thermal anneal", which consists in exposing the exposed surface of the upper layer to the thermal annealing atmosphere for a very short time of less than 2 minutes. The neutral or reducing atmosphere of the annealing chamber is rapidly heated to the processing temperature, which can reach 1200°C,

and then cooled in the course of heating/cooling ramps that can exceed 50°/s. During this treatment, the substrate is held by way of its rear face in the furnace chamber, on a plurality of tips of a support. However, the applicant has
5 observed that this type of anneal generates lines or planes of dislocations at the points where the substrate is in contact with the support. These lines or planes of dislocations originate from thermal stresses and gravitational forces that this substrate is subject to during
10 the very rapid temperature changes that it undergoes. They sometimes make the substrate unsuitable for use in the subsequent microelectronic component manufacturing steps or, at the very least, can result in the formation of non-functional components if the latter are disposed in line
15 with these defects.

As an alternative to the rapid anneal, during the step of finishing the preparation of the substrate it is possible to apply a long anneal, often designated "batch anneal" in the
20 field, since the substrates are generally placed in the furnace chamber in batches, in a horizontal or vertical arrangement. The atmosphere in the chamber is progressively increased, in gentle ramps of a few degrees per minute, in order to reach a treatment temperature typically of around
25 1100°C. The treatment is continued at this temperature for an extended period of time, from around a few minutes to several hours. The gentleness of the ramps makes it possible to limit the thermal stresses to which the substrate is subjected and limits the appearance of the lines or planes
30 of dislocations observed at the end of a rapid heat treatment.

The applicant has observed, as reported in the graph of Figure 1, that it was possible to compensate for the bow of the substrate (on the ordinate axis in this graph), which
5 was caused by the bow of the support substrate after the oxidation of the trapping layer, by exposing the substrate during the finishing step to a high temperature (abscissa axis in the graph) of strictly greater than 1050°C in order to decrease this bow below 40 micrometres and approaching
10 1100°C in order to obtain a bow of below 30 micrometres. In the graph of Figure 1, the data collected at 1050°C, 1075°C and 1100°C were obtained after long anneals, and the data collected at 1200°C were obtained after rapid anneals.

15 The applicant has also observed that the roughness of the exposed surface of the upper layer of the substrate had a tendency to worsen with the rise in temperature if the dielectric layer (formed by oxidation of the trapping layer of the support) has a thickness greater than 200 nm. This is
20 shown by the measurements reported in the graph in Figure 2, which reports the roughness of the exposed surface of the upper layer (measured by atomic force on a field of measurement of 30 micrometres by 30 micrometres) in the centre (reference "C") and at the edge (reference "B") for
25 increasing annealing temperatures. These anneals were conducted on final substrates each having a dielectric layer buried 400 nm deep, obtained by oxidation of the trapping layer of the support substrate as was mentioned above. In this case, it is observed that the roughness tends to
30 increase almost exponentially with the annealing temperature. It appears that the stack forming the substrate

becomes thermally unstable if the dielectric layer has a high thickness of greater than 200 nm, this instability causing the state of the free surface of the substrate to deteriorate. The finishing heat treatment causes this thermal instability, possibly owing to relaxations of stresses in this stack, this relaxation manifesting itself in increased roughness on the surface of the upper layer.

It thus does not appear to be easy to obtain a final substrate of the semiconductor-on-insulator type comprising a thick dielectric layer with a thickness greater than 200 nm, exhibiting both low roughness (less than the limit indicated in a passage above) and a small bow, less than for example 60 micrometres and advantageously without an excessive amount of planes or lines of dislocations.

OBJECT OF THE INVENTION

One aim of the invention is to propose a solution to this problem. More specifically, the invention proposes a substrate comprising a buried dielectric layer more than 2000 nm thick, which exhibits both low roughness and a small bow. The invention also proposes a method for preparing such a substrate.

BRIEF DESCRIPTION OF THE INVENTION

In order to achieve this aim, the subject matter of the invention proposes a method for preparing a final substrate

comprising a thick buried dielectric layer, the method comprising:

- a step of preparing a support substrate comprising an electric-charge trapping layer disposed on a base substrate;
- a step of forming a dielectric layer having a thickness greater than 200 nm on the electric-charge trapping layer;
- a step of transferring an upper layer comprising a semiconductor material to the dielectric layer;
- a step of finishing the exposed face of the upper layer.

According to the invention, the step of forming the dielectric layer is carried out by high-density plasma chemical vapour deposition and the finishing step comprises a first anneal performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration greater than 30 minutes.

Surprisingly, this method makes it possible to obtain a final substrate exhibiting both reduced bow and a satisfactory surface state.

According to other advantageous and non-limiting features of the invention, which may be implemented alone or in any technically feasible combination:

- the step of forming the dielectric layer comprises, after the high-density plasma chemical vapour deposition of the dielectric layer, a densifying anneal of the support substrate;

- the densifying anneal is carried out in a neutral atmosphere at a temperature below 1000°C and for a duration less than 1 h;
- 5 • the finishing step comprises a thinning of the upper layer before and/or after the first anneal;
- the thinning is carried out by sacrificial oxidation;
- 10 • the finishing step comprises a second anneal, the second anneal being performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration less than 2 minutes;
- 15 • the neutral or reducing atmosphere of the first anneal comprises or is made up of argon;
- the step of forming the dielectric layer does not include polishing the exposed face of the dielectric layer;
- 20 • the semiconductor material is silicon;
- the dielectric layer is made of silicon dioxide;
- 25 • the dielectric layer has a thickness greater than or equal to 400 nm;
- the step of transferring the upper layer comprises a step of implanting species referred to as "light" species in
30 a donor substrate so as to form a weakened plane there,

joining the donor substrate to the support substrate, and
fracturing the donor substrate in the weakened plane.

5 According to another aspect, the invention proposes a final
substrate comprising the following in succession and in
contact with one another: an upper layer made of
semiconductor material, a dielectric layer having a
thickness greater than 200 nm, an electric-charge trapping
layer, and a base substrate.

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According to the invention, the final substrate has an
exposed surface of the layer made of semiconductor material
having a roughness less than 0.3 nm measured in root mean
square terms over a field of 30 micrometres by 30 micrometres
15 and a bow less than 60 micrometres, preferably less than 40
micrometres.

According to other advantageous and non-limiting features of
this other aspect of the invention, which may be implemented
20 alone or in any technically feasible combination:

- the upper layer is made of silicon;
- the dielectric layer is made of silicon oxide;
- 25 • the final substrate takes the form of a disc with a
diameter of 300 mm or more;
- the final substrate has a total length of planes or lines
30 of dislocations, measured by deflectometry, of less than
20 mm.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Other features and advantages of the invention will become apparent from the following detailed description of the invention, which is given with reference to the appended figures, in which:

10 [Fig. 1]

Figure 1 shows a graph linking the bow of a substrate of the silicon-on-insulator type with the temperature of an anneal applied during a step of finishing the preparation of this substrate;

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[Fig. 2]

Figure 2 shows a graph linking, for a dielectric layer buried 400 nm deep, the roughness of the exposed surface of the upper layer of a final substrate with the temperature of an
20 anneal applied during a step of finishing the preparation of this substrate;

[Fig. 3]

Figure 3 shows a substrate according to the invention;

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[Fig. 4a]

[Fig. 4b]

[Fig. 4c]

[Fig. 4d]

30 Figures 4a, 4b, 4c, 4d show a method for preparing a final substrate according to the present invention;

[Fig. 5a]

[Fig. 5b]

Figures 5a, 5b show bow and roughness measurements,
5 respectively, taken during experiments that made it possible
to arrive at the invention;

[Fig. 6]

Figure 6 illustrates the advantage afforded by the use of a
10 "long" anneal, rather than a "rapid" anneal, in terms of
defects of the dislocation type in a manufacturing method
according to the invention.

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DETAILED DESCRIPTION OF THE INVENTION

With reference to Figure 3, a substrate S of one embodiment
comprises a base substrate 3, an electric-charge trapping
layer 2 (designated "trapping layer" in the rest of this
20 description) disposed on the base substrate 3, a dielectric
layer 4 disposed on and in direct contact with the trapping
layer 2, and an upper layer 5 disposed on the dielectric
layer 4. The base substrate 3 provided with the charge
trapping layer and with the dielectric layer 4 forms a
25 support substrate 1 of the final substrate S.

The substrate S (and therefore the support substrate 1) can
take the form of a wafer, for example in the shape of a disc
with a diameter of 300 mm. The substrate has a bow less than
30 60 micrometres, preferably less than 40 micrometres, to make

it compatible with the subsequent component manufacturing steps.

5 The base substrate 3 has a thickness of several hundreds of microns. Preferably, the base substrate 3 exhibits a high resistivity of greater than 100 or 1000 ohm.cm, and more preferably still greater than 3000 ohm.cm. This limits the density of charges, i.e. holes or electrons, which are able to move in the base substrate 3 and therefore degrade the
10 radiofrequency performance of the final substrate S. However, the invention is not limited to a base substrate 3 exhibiting such a resistivity, and it also affords advantages in terms of RF performance when the base substrate 3 exhibits a more typical resistivity of less than 1000 ohm.cm, of
15 around a few hundred ohm.cm, or 100 ohm.cm or less.

For reasons of availability and cost, the base substrate 3 is preferably made of silicon, and in particular of monocrystalline silicon. It may, for example, be a CZ
20 substrate containing a small amount of interstitial oxygen, this type of substrate, as is well known per se, having a resistivity that may be greater than 1000 ohm.cm. The base substrate 3 may alternatively be formed from another material: this material may, for example, be sapphire,
25 silicon carbide, silicon-germanium, III-V materials, glass, etc. It may alternatively also be a more standard monocrystalline CZ substrate, the resistivity of which is less than 1000 ohm.cm, or else a CZ substrate containing a high or medium amount of interstitial oxygen, which may be
30 n- or p-doped and which has a resistivity that may be around 500 ohm.cm or less.

The support substrate 1 also has a trapping layer 2, disposed on and in direct contact with the base substrate 3. The trapping layer 2 has a resistivity greater than 500 ohm.cm and preferably greater than 1000 ohm.cm, and even more preferably greater than 10 kohm.cm. As is well known per se, the function of the trapping layer is to trap charge carriers that may be present in the support 1 and to limit their mobility. This is notably the case if the substrate S comprises a semiconductor structure which emits an electromagnetic field that penetrates into the support substrate 1 and is therefore able to interact with these charges and make them mobile. The trapping layer 2 has a thickness typically of between 1 micron and 15 microns, or even 20 microns.

The trapping layer 2 may, in general, be made up of a non-monocrystalline semiconductor layer exhibiting structural defects such as dislocations, grain boundaries, amorphous zones, interstices, inclusions, pores, etc. These structural defects form traps for any charges flowing through the material, for example at the site of incomplete or dangling chemical bonds. Conduction is thus prevented in the trapping layer, which consequently has a high resistivity.

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For the same reasons of availability and cost that have already been mentioned, the trapping layer 2 is preferably made of polycrystalline silicon. However, it may be made up of or comprise another polycrystalline semiconductor material. Of course, this charge trapping layer 2 may be formed by a technique other than that involving a layer

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formed from polycrystalline silicon. This layer may also comprise carbon or be made up of or comprise silicon carbide or an alloy of silicon and carbon, for example in the form of interlayers inserted in a thickness of polycrystalline silicon. When the trapping layer 2 is made up of silicon carbide or an alloy of silicon and carbon, its thickness is preferably between a few nm (for example 2 nm) and a few tens of nm (for example 50 nm). Alternatively, the electric traps may be formed in the layer 2 by ion bombardment with relatively heavy species (for example argon) in a surface portion of the base substrate 3 in order to create crystal defects there that are able to trap electric charges. It is also possible to envisage a charge trapping layer 2 formed from a porous material, for example by making a surface portion of the base substrate 3 porous if the base substrate is made of silicon. The trapping layer may also comprise a silicon-rich oxide having an atomic concentration of silicon of between 50% and 99.9%. This silicon-rich oxide may also comprise nitrogen. It may also comprise inclusions of crystalline silicon having a size less than 10 nm, and preferably less than 5 nm. As an alternative, it may have a polycrystalline form and comprise amorphous inclusions.

In any case, the trapping layer 2 exhibits a high resistivity of greater than 500 ohm.cm. To that end, the trapping layer 2 is not intentionally doped, i.e. it has a charge carrier dopant concentration of less than 10^{14} atoms per cubic centimetre. It may be rich in nitrogen or carbon in order to improve its resistivity characteristic.

Returning to the general description of Figure 3, the support substrate 1 also comprises a dielectric layer 4 directly disposed on the trapping layer 2. By way of example, the dielectric layer 4 may be made up of or comprise silicon dioxide or silicon nitride. It may also be a stack of these materials. The thickness of the dielectric layer 4 may be usually between 10 nm and 10 microns, but in the context of the present description, this layer has a high thickness of greater than 200 nm, and preferably between 200 nm and 1000 nm.

The substrate S comprises an upper layer 5, on and in contact with the dielectric layer 4 of the support substrate 1. The thin layer is usually made of monocrystalline silicon, but it could be made of any other material depending on the nature of the device intended to be formed there. When the substrate S is intended to receive integrated semiconductor components, in the fields of electronics and photonics, the thin layer 5 may thus be composed of monocrystalline silicon or any other monocrystalline semiconductor material such as germanium, silicon-germanium, or silicon carbide.

In all cases, and irrespective of the nature of the upper layer, it has very little roughness, and its exposed surface exhibits a roughness less than 0.3 nm measured in root mean square terms over a field of 30 micrometres by 30 micrometres.

The ability to provide a (more than 200 nm) thick buried dielectric substrate exhibiting both low surface roughness and a small bow forms a very notable aspect of the present

invention. Furthermore, this substrate has a low density of planes or lines of dislocations. These planes or lines of dislocations can be measured by an inspection instrument implementing a deflectometry technique, as presented for example in document US7812942. It is generally desired to minimize the total length of these planes or lines of dislocations, for example below the threshold value of 20 mm, this indeed being the case for a substrate according to the invention.

Preparation of the substrate

A method for preparing the substrate shown in Figures 4a to 4d will now be presented.

In a first, preparation step shown in Figure 4a, the support substrate 1 is prepared. The manufacture of the trapping layer 2, if it is made of polycrystalline silicon or formed from a silicon-rich oxide, on the base substrate 3 can be carried out with industry-standard deposition instruments. This may involve RPCVD (remote plasma-enhanced chemical vapour deposition) or PECVD (plasma-enhanced chemical vapour deposition). It may also involve LPCVD (low-pressure chemical vapour deposition). However, as seen above, the formation of the trapping layer on or in the base substrate 3 may be realized in many other ways, for example by implanting heavy species or by making a surface layer of the base substrate 3 porous.

Optionally, during this preparation step, a thin dielectric layer may have been formed on the base substrate 3, for example by oxidation or deposition of a thickness of oxide, before forming the trapping layer 2 there.

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In a second step of the preparation method, this step being shown in Figure 4b, the dielectric layer 4 having a thickness greater than 200 nm is formed. Very generally, there are numerous options for forming this dielectric layer 4 such that it is buried in the substrate S at the end. The dielectric layer may be formed on the support substrate 1 by deposition or by treatment (oxidation, for example) of the trapping layer 2. It may also be formed on a substrate referred to as "donor" substrate, which provides the upper layer 5. According to the present invention, and for reasons which will be made apparent in the rest of this description, the dielectric layer 4 is by produced on the trapping layer 3 by high-density plasma chemical vapour deposition. This technique simultaneously implements the deposition and the ion sputtering of this dielectric layer 4. It notably has the advantage of providing a thick layer of low roughness, and therefore it is possible for its formation step to not include any smoothing treatment, such as polishing. After this step of forming the dielectric layer, the support substrate 1 is provided. This support substrate may have a considerable bow, sometimes greater than 60 micrometres when the support substrate 1 has a circular shape and a diameter of 300 mm.

It should be noted that the method for preparing the support substrate 1 may also incorporate a step of annealing the

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dielectric layer 4. This anneal, referred to as a densifying anneal, is advantageously performed in a neutral atmosphere. It is carried out at a temperature higher than the temperature of deposition of the dielectric layer 4, and preferably lower than 1000°C, for a relatively short period of time of less than 1 h, for example 30 minutes.

Continuing the description of the method for manufacturing the final substrate S, the method comprises, in a third step following the second step, the transfer of the upper layer 5 comprising a semiconductor material to the dielectric layer 4. As is well known per se, this transfer can be achieved by joining a free face of a donor substrate 1' to the support substrate 1, preferably by molecular bonding. Since the dielectric layer 4 was formed on the support substrate 1 beforehand, it is not necessary for the donor substrate 1' itself to be provided with such a dielectric layer. It is nevertheless possible to envisage that this donor substrate is provided with a fine thickness of dielectric (for example less than 150 nm). With preference, however, the donor substrate does not have any intentionally formed dielectric surface layer. The nature of the donor substrate 1' is chosen according to the desired nature of the upper layer 5, as has already been described in a previous section of this description. It may therefore be a substrate formed from a monocrystalline semiconductor, for example silicon.

After this joining step, the donor substrate has its thickness reduced so as to form the upper layer 5, as shown in Figure 4d. This reduction step may be realized by mechanical and/or chemical thinning. With preference,

however, the thickness of the donor substrate 1' is reduced by fracture in a weakened plane made beforehand, for example according to the principles of Smart Cut TM technology. In accordance with the principles of this technology, the transfer of the upper layer 5 comprises a step of implanting species referred to as "light" species, for example hydrogen and/or helium ions, in the donor substrate 1' so as to form a weakened plane there. This weakened plane defines, with the free surface of the donor substrate, the upper layer 5 which will be transferred. After the donor substrate 1' has been joined to the support substrate 1, the donor substrate is fractured in the weakened plane, by applying a force of mechanical or thermal origin.

After this thinning, or preferably fracturing, step, steps for finishing the thin layer 5, such as a heat treatment under a reducing or neutral atmosphere, and sacrificial oxidation may be carried out after the thickness reduction step.

Very surprisingly, the applicant has discovered that it was possible to obtain both a reduced bow and a satisfactory surface state if the dielectric layer 4 is formed by high-density plasma chemical vapour deposition and if the finishing step comprises an anneal performed in a neutral or reducing atmosphere at a temperature above 1050°C for a period of time greater than 30 minutes.

Figures 5a and 5b thus show the measured characteristics of the bow of the final substrate S (Figure 5a) and of the roughness of the exposed surface of the upper layer 5 (Figure

5b; this roughness measurement, expressed in nm, being taken by atomic force over a field of measurement of 30 micrometres by 30 micrometres) of a substrate prepared according to the method which has just been set out. It can be seen in Figure 5a that it is possible to reduce the bow of the final substrate S by increasing the temperature of the anneal of the finishing step. If this anneal takes the substrate to 1050°C, this bow is around 55 micrometres, and this is already very satisfactory. It will be noted that the results at 1200°C that were obtained using a rapid anneal also make it possible to reduce the bow of the substrate, but can give rise to dislocation-type defects, as was mentioned in the introduction of this application.

It can also be seen in Figure 5b that, unexpectedly, the measured roughness of the upper layer 5 after the anneal of the finishing step has been applied is stable as this temperature rises and is at a level less than 0.3 nm measured in root mean square terms, and this is also very satisfactory, both at the edge of the substrate (mark "B") and in its centre (mark "C"). It will be recalled that the applicant's preparatory observations, reported in Figure 2, showed a roughness of the exposed surface of this upper layer 5 that increases with the increase in temperature.

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A preparation method according to the invention therefore utilizes these results to propose various finishing sequences for a finishing step. In all these possible sequences, there is at least one anneal, designated "first anneal", this first anneal being carried out in a neutral or reducing atmosphere at a temperature above 1050°C for a

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period of time greater than 30 minutes. In all these cases, the dielectric layer 4, buried in the final substrate, was also obtained by high-density plasma chemical vapour deposition on the charge trapping layer 2.

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The finishing step may thus comprise at least one step of thinning the upper layer 5. This at least one thinning step may be carried out before and/or after the first anneal. The finishing sequence performed during the finishing step may thus correspond to a thinning-annealing or annealing-thinning or else thinning-annealing-thinning sequence. This thinning of the layer can notably be carried out by sacrificial oxidation (which is to say the oxidation of a sacrificial thickness of this layer, followed by the removal of this oxidized thickness) of the upper layer.

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Furthermore, the finishing step may comprise anneals other than the first anneal already described. In one embodiment variant, the finishing sequence may thus incorporate comprises a rapid second anneal, this second anneal being performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration less than 2 minutes. The second anneal can be carried out before or after the first anneal.

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The neutral or reducing atmosphere used during the first anneal and, as the case may be, during the second anneal is preferably composed mainly or exclusively of argon.

The temperature of the first anneal may be chosen preferably in the range of 1050°C to 1100°C, in order to not adversely

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affect the quality of the trapping layer 2. An excessive thermal budget during the finishing step could effectively result in modifying its crystallinity and its electrical effectiveness. To further improve the smoothing effect of this first anneal, even for the low end of the preferred temperature range, the equipment in which this anneal is performed can follow the teachings of document EP3011590B1.

To avoid generating dislocation-type defects in the final substrate, it will be preferred to avoid introducing a rapid anneal into the finishing sequence, although this is not entirely ruled out.

Figure 6 illustrates the advantage afforded by the use of a "long" anneal solely in the finishing sequence, rather than a "rapid" anneal in terms of dislocation-type defects. The left-hand part of this figure presents a map of the dislocations present in a final substrate for which the finishing sequence comprises an anneal performed in a neutral or reducing atmosphere at a temperature above 1050°C for a period of time greater than 30 minutes, still without any rapid annealing. This left-hand part shows the absence, or virtually the absence, of such defects.

The right-hand part of this figure presents a map of the dislocations present in a final substrate that has received a rapid heat treatment. The difference, in terms of defectiveness, compared to the left-hand part will be readily noted.

These maps of dislocations can be prepared by an inspection instrument implementing a deflectometry technique, as presented for example in document US7812942.

5 Irrespective of the finishing sequence used, the preparation method that has just been described makes it possible to propose a final substrate comprising the following in succession and in contact with one another: an upper layer
5 made of semiconductor material, for example made of
10 silicon, a dielectric layer having a thickness greater than 200 nm, an electric-charge trapping layer, and a base substrate. The dielectric layer may notably have a thickness greater than or equal to 400 nm. The exposed surface of the upper layer made of semiconductor material of this final
15 substrate has a roughness less than 0.3 nm measured in root mean square terms over a field of 5 micrometres by 5 micrometres and a bow less than 60 micrometres, preferably less than 40 micrometres. Advantageously, this final substrate has a total length of planes or lines of
20 dislocations of less than 20 mm.

Of course, the invention is not limited to the embodiments described, and modifications may be applied thereto without departing from the scope of the invention as defined by the
25 claims.

CLAIMS

1. Method for preparing a final substrate (S) comprising a thick buried dielectric layer (4), the method comprising:
 - 5 - a step of preparing a support substrate (1) comprising an electric-charge trapping layer (2) disposed on a base substrate (3);
 - a step of forming the dielectric layer (4) having a thickness greater than 200 nm on the electric-charge trapping layer (2);
 - 10 - a step of transferring an upper layer (5) comprising a semiconductor material to the dielectric layer (4);
 - a step of finishing the exposed face of the upper layer (5);
- 15 the preparation method being characterized in that the step of forming the dielectric layer (4) is carried out by high-density plasma chemical vapour deposition and in that the finishing step comprises a first anneal performed in a neutral or reducing atmosphere at a temperature above 1050°C
- 20 for a duration greater than 30 minutes.
2. Preparation method according to the preceding claim, wherein the step of forming the dielectric layer (4) comprises, after the high-density plasma chemical vapour
- 25 deposition of the dielectric layer, a densifying anneal of the support substrate.
3. Preparation method according to the preceding claim, wherein the densifying anneal is carried out in a neutral
- 30 atmosphere at a temperature below 1000°C and for a duration less than 1 h.

4. Preparation method according to one of the preceding claims, wherein the finishing step comprises a thinning of the upper layer (5) before and/or after the first anneal.

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5. Preparation method according to one of the preceding claims, wherein the finishing step comprises a second anneal, the second anneal being performed in a neutral or reducing atmosphere at a temperature above 1050°C for a duration less than 2 minutes.

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6. Preparation method according to one of the preceding claims, wherein the neutral or reducing atmosphere of the first anneal comprises or is made up of argon.

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7. Preparation method according to one of the preceding claims, wherein the step of forming the dielectric layer (4) does not include polishing the exposed face of the dielectric layer (4).

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8. Preparation method according to one of the preceding claims, wherein the semiconductor material of the upper layer (5) is silicon.

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9. Preparation method according to one of the preceding claims, wherein the dielectric layer (4) is made of silicon dioxide.

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10. Preparation method according to one of the preceding claims, wherein the dielectric layer (4) has a thickness greater than or equal to 400 nm.

11. Method according to one of the preceding claims, wherein the step of transferring the upper layer comprises a step of implanting species referred to as "light" species in a donor substrate (1') so as to form a weakened plane there, joining
5 the donor substrate to the support substrate (1), and fracturing the donor substrate in the weakened plane.

12. Final substrate (S) comprising the following in succession and in contact with one another: an upper layer
10 (5) made of semiconductor material, a dielectric layer (4) having a thickness greater than 200 nm, an electric-charge trapping layer (2), and a base substrate (3), the final substrate (S) being characterized in that it has a bow less than 60 micrometres, preferably less than 40 micrometres,
15 and in that an exposed surface of the upper layer (5) exhibits a roughness less than 0.3 nm measured in root mean square terms over a field of 30 micrometres by 30 micrometres.

20 13. Final substrate (S) according to the preceding claim, wherein the upper layer (5) is made of silicon.

14. Final substrate (S) according to one of the two preceding claims, wherein the dielectric layer (4) is made
25 of silicon oxide.

15. Final substrate (S) according to one of the 3 preceding claims, having a total length of planes or lines of dislocations, measured by deflectometry, of less than 20 mm.