

METHODS AND APPARATUS FOR BARRIER INTERFACE PREPARATION OF COPPER INTERCONNECT

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BACKGROUND

[1] Integrated circuits use conductive interconnects to wire together the individual devices on a semiconductor substrate, or to communicate externally to the integrated circuit. Interconnect metallization for vias and trenches may include aluminum alloys and copper. As device geometry continued to scale down to 65-nm-node technology and sub-65-nm technology, the requirement of continuous barrier/seed layer with good step coverage along high aspect ratio geometry to provide void free copper filling becomes challenging. The motivation to go to ultra thin and conformal barrier in 65-nm-node or sub-65-nm-technology is to reduce the barrier's impact on via and line resistance. However, poor adhesion of copper to the barrier layer could cause delamination between the barrier layer and copper during processing or thermal stressing that poses a concern on electro-migration and stress-induced voiding.

[2] In view of the foregoing, there is a need for systems and processes that enable deposition of a thin and conformal barrier layer, and a copper layer in the copper interconnect with good electro-migration performance and with reduced risk of stress-induce voiding of copper interconnect.

SUMMARY

[3] Broadly speaking, the embodiments fill the need enabling deposition of a thin and conformal barrier layer, and a copper layer in the copper interconnect with good electro-migration performance and with reduced risk of stress-induce voiding of copper interconnect. Electromigration and stress-induced voiding are affected by the adhesion between the barrier layer and the copper layer, which can be improved by making the barrier layer metal-rich prior copper deposition and by limiting the amount of oxygen the barrier layer is exposed prior to copper deposition. Alternatively, a functionalization layer can be deposited over the barrier layer to enable the copper layer being deposit in the copper interconnect. The

functionalization layer forms strong bonds with barrier layer and with copper to improve adhesion property between the two layers. The functionalization layer can also merely enable the deposition of copper over the barrier layer and be replaced by the copper layer. It should be appreciated that the present invention can be implemented in numerous ways, including as a solution, a method, a process, an apparatus, or a system. Several inventive embodiments of the present invention are described below.

[4] In one embodiment, a method of preparing a substrate surface of a substrate to deposit a functionalization layer over a metallic barrier layer of a copper interconnect to assist deposition of a copper layer in the copper interconnect in an integrated system in order to improve electromigration performance of the copper interconnect is provided. The method includes depositing the metallic barrier layer to line the copper interconnect structure in the integrated system, wherein after depositing the metallic barrier layer, the substrate is transferred and processed in controlled environment to prevent the formation of metallic barrier oxide. The method also includes depositing the functionalization layer over the metallic layer in the integrated system. The method further includes depositing the copper layer in the copper interconnect structure in the integrated system after the functionalization layer is deposited over the metallic barrier layer.

[5] In another embodiment, an integrated system for processing a substrate in controlled environment to enable deposition of a functionalization layer over a metallic barrier layer of a copper interconnect to improve electromigration performance of the copper interconnect is provided. The system includes a lab-ambient transfer chamber capable of transferring the substrate from a substrate cassette coupled to the lab-ambient transfer chamber into the integrated system. The system also includes a vacuum transfer chamber operated under vacuum at a pressure less than 1 Torr. The method further includes a vacuum process module for depositing the metallic barrier layer, wherein the vacuum process module for depositing the metallic barrier layer is coupled to the vacuum transfer chamber, and is operated under vacuum at a pressure less than 1 Torr. In addition, the method includes a controlled-ambient transfer chamber filled with an inert gas selected from a group of inert gases, and a deposition process module used to deposit the functionalization layer on the surface of the metallic barrier layer, wherein the deposition process module used to deposit the functionalization layer is coupled to the controlled-ambient transfer chamber.

[6] Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[7] The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[8] Figures 1A-1D show cross sections of a dual-damascene interconnect structure at various stages of interconnect processing.

[9] Figures 2A-2C show cross sections of a metal line structure at various stages of interconnect processing.

[10] Figure 3A shows an exemplary process flow of interconnect processing.

[11] Figure 3B shows an exemplary integrated system used to process a substrate using a process flow of Figure 3A.

[12] Figures 4A-4D show cross sections of a metal line structure at various stages of interconnect processing to incorporate a functionalization layer.

[13] Figures 5A-5E show cross sections of an interconnect structure at various stages of interconnect processing to incorporate a functionalization layer.

[14] Figure 6A shows an exemplary process flow of interconnect processing that incorporates a functionalization layer.

[15] Figure 6B shows an exemplary integrated system used to process a substrate using a process flow of Figure 6A.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[16] Several exemplary embodiments for improved metal integration techniques that remove interfacial metal oxide by reduction or add an adhesion-promoting layer to improve interface adhesion and to lower the resistivity of metal interconnect are provided. It should be appreciated that the present invention can be implemented in numerous ways, including a process, a method, an apparatus, or a system. Several inventive embodiments of the present

invention are described below. It will be apparent to those skilled in the art that the present invention may be practiced without some or all of the specific details set forth herein.

[17] Figure 1A shows an exemplary cross-section of an interconnect structure(s) after being patterned by using a dual damascene process sequence. The interconnect structure(s) is on a substrate 50 and has a dielectric layer 100, which was previously fabricated to form a metallization line 101 therein. The metallization line is typically fabricated by etching a trench into the dielectric 100 and then filling the trench with a conductive material, such as copper.

[18] In the trench, there is a barrier layer 120, used to prevent the copper material 122, from diffusing into the dielectric 100. The barrier layer 120 can be made of physical vapor deposition (PVD) tantalum nitride (TaN), PVD tantalum (Ta), atomic layer deposition (ALD) TaN, or a combination of these films. Other barrier layer materials can also be used. A barrier layer 102 is deposited over the planarized copper material 122 to protect the copper material 122 from premature oxidation when via holes 114 are etched through overlying dielectric materials 104, 106 to the barrier layer 102. The barrier layer 102 is also configured to function as a selective etch stop. Exemplary barrier layer 102 materials include silicon nitride (SiN) or silicon carbide (SiC).

[19] A via dielectric layer 104 is deposited over the barrier layer 102. The via dielectric layer 104 can be made of an organo-silicate glass (OSG, carbon-doped silicon oxide) or other types of dielectric materials, preferably with low dielectric constants. Exemplary silicon dioxides can include, a PECVD un-doped TEOS silicon dioxide, a PECVD fluorinated silica glass (FSG), a HDP FSG, OSG, porous OSG, etc. and the like. Commercially available dielectric materials including Black Diamond (I) and Black Diamond (II) by Applied Materials of Santa Clara, California, Coral by Novellus Systems of San Jose, Aurora by ASM America Inc. of Phoenix, Arizona, can also be used. Over the via dielectric layer 104 is a trench dielectric layer 106. The trench dielectric layer 106 may be a low K dielectric material, such as a carbon-doped oxide (C-oxide). The dielectric constant of the low K dielectric material can be about 3.0 or lower. In one embodiment, both the via and trench dielectric layers are made of the same material, and deposited at the same time to form a continuous film. After the trench dielectric layer 106 is deposited, the substrate 50 that holds

the structure(s) undergoes patterning and etching processes to form the vias holes 114 and trenches 116 by known art.

[20] Figure 1B shows that after the formation of vias holes 114 and trenches 116, a barrier layer 130 and a copper layer 132 are deposited to line and fill the via holes 114 and the trenches 116. The barrier layer 130 can be made of tantalum nitride (TaN), tantalum (Ta), Ruthenium (Ru), or a hybrid combination of these materials. While these are the commonly considered materials, other barrier layer materials can also be used. Barrier layer materials may be other refractory metal compound including but not limited to titanium (Ti), tungsten (W), zirconium (Zr), hafnium (Hf), molybdenum (Mo), niobium (Nb), vanadium (V), ruthenium (Ru) and chromium (Cr), among others.

[21] A copper film 132 is then deposited to fill the via holes 114 and the trenches 116, as shown in Figure 1C. In one embodiment, the copper film 132 includes a thin copper seed layer 131 underneath. In one embodiment, the thickness of the thin copper seed layer is between about 5 angstroms to about 300 angstroms.

[22] Barrier layer, such as Ta, TaN or Ru, if exposed to air for extended period of time, can form Ta_xO_y (Tantalum oxide), TaO_xN_y (Tantalum oxynitride), or RuO_2 (Ruthenium oxide). Electroless deposition of a metal layer on a substrate is highly dependent upon the surface characteristics and composition of the substrate. Electroless plating of copper on a Ta, TaN, or Ru surface is of interest for both seed layer formation prior to electroplating, and selective deposition of Cu lines within lithographically defined pattern(s). One concern is the inhibition of the electroless deposition process by atomically thin native metal oxide layer formed in the presence of oxygen (O_2).

[23] In addition, copper film does not adhere to the barrier oxide layer, such as tantalum oxide, tantalum oxynitride, or ruthenium oxide, as well as it adheres to the pure barrier metal or barrier-layer-rich film, such as Ta, Ru, or Ta-rich TaN film. Ta and/or TaN barrier layers are only used as examples. The description and concept apply to other types of barrier metals, such as Ta or TaN capped with a thin layer of Ru. As described above, poor adhesion can negatively affect the EM performance. In addition, the formation tantalum oxide or tantalum oxynitride on the barrier layer surface can increase the resistivity of the barrier layer. Due to these issues, it is desirable to use the integrated system to prepare the

barrier/copper interface to ensure good adhesion between the barrier layer and copper and to ensure low resistivity of the barrier layer.

[24] Figure 1B shows that the barrier layer 130 is a single layer deposited either by ALD or PVD. Alternatively, the barrier layer 130 can be deposited by an ALD process to deposit a first barrier layer 130_I, such as TaN, which is followed by a PVD second barrier layer 130_{II}, such as Ta, as shown in Figure 1D.

[25] In addition to dual-damascene interconnect structures, copper interconnect can also be applied to metal lines (or M1 lines) over contacts. Figure 2A shows an exemplary cross-section of a metal line structure after being patterned by a dielectric etch and being removed of photoresist. The metal line structure(s) is on a substrate 200 and has a silicon layer 110, which was previously fabricated to form a gate structure 105 with a gate oxide 121, spacers 107 and a contact 125 therein. The contact 125 is typically fabricated by etching a contact hole into the oxide 103 and then filling the contact hole with a conductive material, such as tungsten. Alternative materials may include copper, aluminum or other conductive materials. The barrier layer 102 is configured to function as a selective trench etch stop. The barrier layer 102 can be made of materials such as silicon nitride (SiN) or silicon carbide (SiC).

[26] A metal line dielectric layer 106 is deposited over the barrier layer 102. The dielectric materials that can be used to deposit 106 have been described above. After the deposition of dielectric layer 106, the substrate is patterned and etched to create metal trenches 106. Figure 2B shows that after the formation of metal trenches 116, a metallic barrier layer 130 is deposited to line metal trench 116. Figure 2C shows that after the barrier layer 130 is deposited, a copper layer 132 is deposited over the barrier layer 130. Similar to the dual-damascene interconnect structures, the barrier layer 130 can be made of tantalum nitride (TaN), tantalum (Ta), Ru, or a combination of these films. A copper film 132 is then deposited to fill the metal trench 116.

[27] As described above for dual-damascene structures, barrier layer, such as Ta, TaN or Ru, if exposed to air for extended period of time, can form Ta_xO_y (Tantalum oxide), TaO_xN_y (Tantalum oxynitride), or RuO₂ (Ruthenium oxide). Electroless deposition of a metal layer on a substrate is highly dependent upon the surface characteristics and composition of the substrate. Electroless plating of copper on a Ta, TaN, or Ru surface is of interest for both seed layer formation prior to electroplating, and selective deposition of Cu lines within

lithographically defined pattern(s). As described above, the concern is the inhibition of the electroless deposition process by atomically thin native metal oxide layer formed in the presence of oxygen (O_2). In addition, copper film does not adhere to the barrier oxide layer, such as tantalum oxide, tantalum oxynitride, or ruthenium oxide, as well as it adheres to the pure barrier metal or barrier-layer-rich film, such as Ta, Ru, or Ta-rich TaN film. As described above, poor adhesion can negatively affect the EM performance. The formation of tantalum oxide or tantalum oxynitride on the barrier layer surface can also increase the resistivity of the barrier layer. Due to these issues, it is desirable to use the integrated system to prepare the barrier/copper interface to ensure good adhesion between the barrier layer and copper and to ensure low resistivity of the barrier layer.

[28] Figure 3A shows an embodiment of a process flow 300 of preparing a barrier (or liner) layer surface for electroless copper deposition after the trenches, such as trenches 116 of Figure 2A) have been formed. Forming metal trench interconnect over contact plugs, as shown in figure 2A-2C, is merely used as an example. The concept of the invention can also be used to form dual-damascene interconnect structures over metal trenches, such as the ones shown in Figures 1A-1D, or other applicable interconnect structures. It should be noted, however, that the barrier (or liner) layer may be prepared separately in a non-integrated deposition system, such as an ALD or PVD deposition reactor. In this case, the surface preparation for depositing a thin copper seed layer would not include the metal plug pre-clean and barrier deposition process steps. At step 301, the top surface 124a of the contact plug is cleaned to remove native metal oxide. Metal oxide can be removed by an Ar sputtering process, a plasma process using a fluorine-containing gas, such as NF_3 , CF_4 , or a combination of both, a wet chemical etch process, or a reduction process, for example using a hydrogen-containing plasma. Metal oxide can be removed by a wet chemical removal process in a 1-step or a 2-step wet chemical process sequence. The wet chemical removal process can use an organic acid, such as DeerClean offered by Kanto Chemical Co., Inc. of Japan or a semi-aqueous solvent, such as ESC 5800 offered by DuPont of Wilmington, Delaware, an organic base such as tetramethylammonium chloride (TMAH), complexing amines such as ethylene diamine, diethylene triamine, or proprietary chemistry such as ELD clean and Cap Clean 61, provided by Enthone, Inc. of West Haven, Connecticut. In addition, metal oxides, specifically copper oxide, can be removed using a weak organic acid such as

citric acid, or other organic or inorganic acids can be used. Additionally, very dilute (i.e. <0.1%) peroxide-containing acids, such as sulfuric-peroxide mixtures, can also be used.

[29] At step 303, a barrier layer is deposited. Due to the shrinking metal line and via critical dimension, the barrier layer may be deposited by atomic layer deposition (ALD), depending on the technology node. The thickness of the barrier layer 130 is between about 20 angstroms to about 200 angstroms. As described above, preventing the barrier layer from exposure to oxygen is critical in ensuring that electroless copper is being deposited on the barrier layer with good adhesion between copper and the barrier layer. Once the barrier layer is deposited, the substrate should be transferred or processed in a controlled-ambient environment to limit exposure to oxygen. In one embodiment, the barrier layer is hydrogen-plasma treated to produce a metal-rich surface on the barrier layer, such as Ta, TaN, or Ru, at step 305 to provide a catalytic surface for the subsequent copper seed deposition step. The reducing plasma can include gas, such as hydrogen or ammonia. The reducing plasma can include an inert gas, such as Ar, or He. Step 305 is an optional step, if the barrier surface is metal-rich after barrier layer deposition, such as the deposited barrier layer is a tantalum or ruthenium layer, the surface reduction step is not required. On the other hand, if the barrier layer deposited is a barrier nitride layer, such as TaN, or if the barrier layer is exposed to oxygen, the hydrogen-plasma treatment (or reduction) would be needed. Whether this step is needed or not depends on how metal-rich the surface is.

[30] Afterwards, conformal copper seed is deposited on the barrier surface at step 307, followed by a thick copper gap fill (or bulk fill) process, 308. In one embodiment, the conformal copper seed layer can be deposited by an electroless process. The thick copper bulk fill process can be an electroless deposition (ELD) process or an electrochemical plating (ECP) process. Electroless copper deposition and ECP are well-known wet process. For a wet process to be integrated in a system with controlled processing and transporting environment, the reactor needs to be integrated with a rinse/dryer to enable dry-in/dry-out process capability. In addition, the system needs to be filled with inert gas to ensure minimal exposure of the substrate to oxygen. The electroless deposition process can be carried out in a number of ways, such as puddle-plating, where fluid is dispensed onto a substrate and allowed to react in a static mode, after which the reactants are removed and discarded, or reclaimed. Recently, a dry-in/dry-out electroless copper process has been developed. The

process uses a proximity process head to limit the electroless process liquid in contacting with the substrate surface on a limited region. The substrate surface not under the proximity process head is dry. Further, all fluids used in the process are de-gassed, i.e. dissolved oxygen is removed by commercially available degassing systems.

[31] After copper deposition at steps 307 and 308, the substrate can undergo an optional substrate cleaning at step 309. Post-copper-deposition clean can be accomplished by using a brush scrub clean with a chemical solution, such as a solution containing CP72B supplied by Air Products and Chemical, Inc. of Allentown, Pennsylvania. Other substrate surface cleaning processes can also be used, such as Lam's C3™ or AMC™ (Advanced Mechanical Clean) cleaning technology.

[32] Figure 3B shows an embodiment of a schematic diagram of an integrated system 350 that allows minimal exposure of substrate surface to oxygen at critical steps after barrier surface preparation. In addition, since it is an integrated system, the substrate is transferred from one process station immediately to the next process station, limiting the duration that clean barrier surface is exposed to low levels of oxygen. The integrated system 350 can be used to process substrate(s) through the entire process sequence of flow 300 of Figure 3A.

[33] As described above, the surface preparation for electroless deposition of copper and the optional post-cobalt-alloy deposition processes involves a mixture of dry and wet processes. The wet processes are typically operated near atmosphere, while the dry plasma processes are operated at less than 1 Torr. In addition, after the barrier layer has been deposited, the substrate should be exposed to oxygen as little as possible, which can be achieved by being transferred and processed in controlled environment. Therefore, the integrated system needs to be able to handle a mixture of dry and wet processes. For a wet process to be integrated in a system with controlled processing and transporting environment, the reactor needs to be integrated with a rinse/dryer to enable dry-in/dry-out process capability. In addition, the system needs to be filled with inert gas to ensure minimal exposure of the substrate to oxygen. The integrated system 350 has 3 substrate transfer modules 360, 370, and 380. Transfer modules 360, 370 and 380 are equipped with robots to move substrate 355 from one process area to another process area. The process area could be a substrate cassette, a reactor, or a loadlock. Substrate transfer module 360 is operated under lab ambient. Module 360 interfaces with substrate loaders (or substrate cassettes) 361 to

bring the substrate 355 into the integrated system or to return the substrate to one of the cassettes 361.

[34] As described above in process flow 300, the substrate 355 is brought to the integrated system 350 to deposit barrier layer and copper layer. As described in step 301 of process flow 300, top tungsten surface 124a of contact 125 is etched to remove native tungsten oxide. Once the tungsten oxide is removed, the exposed tungsten surface 124a of Figure 2A needs to be protected from exposure to oxygen. If the removal process is an Ar sputtering process, the reactor 371 is coupled to the vacuum transfer module 370. If a wet chemical etching process is selected, the reactor should be coupled to the controlled-ambient transfer module 1080, not the lab-ambient transfer module 360, to limit exposure of the tungsten surface to oxygen.

[35] Afterwards, the substrate is deposited with a metallic barrier layer, such as Ta, TaN, Ru, or a combination of these films, as described in step 303 of Figure 3A. The barrier layer 130 of Figure 2B can be deposited by an ALD process or a PVD process. In one embodiment, the ALD process is operated at less than 1 Torr. The ALD reactor 373 is coupled to the vacuum transfer module 370. In another embodiment, the deposition process is a high-pressure process using supercritical CO₂ and organo-metallic precursors to form the metal barrier. In yet another embodiment, the deposition process is a physical vapor deposition (PVD) process operating at pressures less than 1 Torr.

[36] The substrate can undergo an optional reduction (hydrogen-plasma treatment) process, for example using a hydrogen-containing plasma, as described in step 305 of Figure 3A. The hydrogen reduction reactor 374 can be coupled to the vacuum transfer module 370. At this stage, the substrate is ready for electroless copper deposition. The electroless copper plating can be performed in an electroless copper-plating reactor 381 to deposit a conformal seed layer. Following the seed layer deposition, copper bulk fill can be performed in the same electroless copper deposition reactor 381 used to deposit the conformal seed layer, but with a different chemistry to achieve bulk fill. Alternatively, copper bulk fill can be performed in a separate ECP reactor 381'.

[37] Before the substrate leaves the integrated system 350, the substrate can optionally undergo a surface cleaning process, which can clean residues from the previous copper deposition process. For example, the substrate cleaning process can be brush clean process.

Substrate cleaning reactor 383 can be integrated with the controlled-ambient transfer module 380. Alternatively, the substrate-cleaning reactor 383 can also be integrated with the lab-ambient transfer module 360. Alternatively, the barrier layer 130 of Figure 2B can be deposited in a process chamber before the substrate 200 is brought into a system for surface treatment and depositing copper. As discussed above, the process flow 300 described in Figure 3A and system 350 described in Figure 3B can also be used to deposit barrier layer and copper for dual damascene structures, as shown in Figures 1A-1D, or other applicable interconnect structures. For dual damascene structures, step 301 in flow 300 is replaced by cleaning top surface of metal line, which is shown as surface 122a of Figure 1A.

[38] As described above, EM performance is affected by the quality of adhesion between copper and the barrier layer. In one embodiment, chemical-grafting chemicals that would selectively bond to conducting or semi-conducting clean surfaces to form a self-assembled monolayer (SAM) of such chemicals on the conducting or semi-conducting clean surfaces. The electro-grafting or chemical-grafting chemical, which is a complexing group and forms a monolayer on a conducting or a semiconducting surface, functionalizes the substrate surface to be deposited with a layer of material over the monolayer with strong bonding between the monolayer and the deposited layer material. Therefore, the monolayer can also be called a functionalization layer. From hereon, the terms self-assembled monolayer and functionalization layer are used interchangeably. Alternatively, the monolayer can be replaced by the deposited material during deposition process. The deposited material forms strong bonding directly with the substrate. The complexing group has one end that forms a covalent bond with the conducting or semiconducting surface. Using Ta as an example of barrier metal for copper interconnect, the complexing group of the functionalization layer has one end forming a strong bond with Ta and another end forming a strong bond with copper, or can be modified to a catalytic site that will bond with copper. For SAM formed by chemical grafting, the chemical-grafting molecules are adsorbed by physisorption and chemisorption from the solution onto solid substrates to bond with the surface and to form ordered and a molecular functionalization layer, which is a self-assembled monolayer.

[39] Figure 4A shows a barrier layer 401 with a barrier surface 410. Figure 4B shows that the barrier surface 410 is deposited with a functionalization layer 402 of the chemical-grafting complexing group 420. The complexing group 420 has two ends, "A" end and "B"

end. “A” end forms a covalent bond with the surface 410 with barrier metal. The complexing group 420 should have an “A” end that would form a covalent bond with the barrier surface, which could be made of materials, such as Ta, TaN, Ru, or other application materials. In one embodiment, the “B” end form a covalent bond with the copper seed layer 403, as shown in Figure 4C. In such embodiment, the “B” end of the complexing group 420 should choose a compound that would form a covalent bond with copper. Alternatively, copper 403’ replaces the entire complexing group 420 to deposit directly on the barrier surface, as shown in Figure 4D. or can be modified to a catalytic site that will bond with copper. The complexing group 420 in the Figure 4D assist the copper in bonding to the barrier surface.

[40] In one embodiment, the “A”-end of the chemical-grafting complexing group is a Lewis acid that interacts (or grafts) with a Lewis base barrier surface to form a bond between the metal and the chemical-grafting chemical (or complexing group). Examples of chemical-grafting complexing (or functional) group includes thiols, silanes, alcohols, organic acids, amine, and pyrrole. Examples of thiols include alkanethiols, such as decanethiol and octadecanethiol, tetraphenylporphines, diphenyl disulfide, aromatic thioacetate, ruthenium (II) tris(2, 2, prime-bipyridine) thiol, thiophenol, 4, 4 prime-dithiodipyridine, naphthalene disulfide, and bis(2-anthraquinyl) disulfide. Examples of silanes include 3-mercaptopropyl trimethoxysilane, γ -methacryloxypropyl triethoxysilane, perfluorooctanoxylpropyl-dimethyl silane, alkyltrichlorosilane, and octadecylsiloxane. An example of alcohols includes octanol. Examples of organic acids include 22-mercapto-1-docosanoic acid, alkanephosphonic acids, and octadecanoic acid. An example of amine includes diaminododecane. Examples of pyrrole include n-phenylpyrrole, and 2,5-dithienylpyrrol triad. The “B” end should be functional groups that contain elements that selectively bond to Cu. Such elements include copper (Cu), cobalt (Co), and ruthenium (Ru).

[41] Figure 5A shows an opening 510 of an interconnect metal structure (metal 1) that is surrounded by a dielectric layer 501. Figure 5B shows that a barrier layer 502 is deposited to line the metal opening 510. The bottom of the metal structure is a contact, which is similar to the contact 125 shown in Figure 2A-2C. The barrier layer can be deposited by ALD, PVD, or other applicable processes. The thickness of the barrier layer is between about 5 angstroms to about 300 angstroms. Figure 5C shows that a functionalization layer 503 of

chemical-grating complexing compound is deposited on barrier layer 502. In one embodiment, the thickness of the functionalization layer 503 is between about 5 angstroms to about 20 angstroms. After the functionalization layer 503 is deposited, a copper seed layer 504 is deposited over the functionalization layer 503, as shown in Figure 5D. After copper seed layer 504 is deposited, copper gap-fill layer 505 is deposited, as shown in Figure 5E.

[42] Figure 6A shows an embodiment of a process flow of preparing the barrier (or liner) layer surface for electroless copper deposition. At step 601, the top surface 125a of contact 125 of Figure 2A is cleaned to remove native metal oxide. Metal oxide can be removed by an Ar sputtering process or a wet chemical etch process. At step 603, a barrier layer is deposited in either an ALD or a PVD system. As described above, preventing the barrier layer from exposure to oxygen is critical in ensuring that electroless copper is being deposited on the barrier layer with good adhesion between copper and the barrier layer. Similarly, for the functionalization layer to be properly deposited on the barrier surface, the barrier surface should be removed of the barrier oxide. Once the barrier layer is deposited, the substrate should be transferred or processed in a controlled-ambient environment to limit exposure to oxygen. The barrier layer is treated by a reducing plasma (i.e. hydrogen-containing) at step 605 to produce a metal-rich layer that will provide a catalytic surface for the subsequent functionalization layer deposition step. The reducing plasma treatment is optional, depending on the composition of the surface. Afterwards, the substrate surface is deposited with a functionalization layer of chemical-grafting complexing compound at step 606. In one embodiment, the chemical-grafting complexing compound is mixed in a solution and the deposition process is a wet process. An optional clean step 607 after the deposition step at 606 may be needed.

[43] Afterwards, a conformal copper seed is deposited on the barrier surface at step 608, followed by a thick copper bulk fill (or gap fill) process, 609. The conformal copper seed layer can be deposited by an electroless process. The thick copper bulk fill (also gap fill) layer can be deposited by an ECP process. Alternatively, the thick bulk fill (also gap fill) layer can be deposited by an electroless process in the same electroless system for conformal copper seed, but with a different chemistry.

[44] After the substrate is deposited with conformal copper seed at step 608, and thick Cu bulk fill by either an electroless or electro-plating process at step 609, the next process step

610 is an optional substrate-cleaning step to clean any residual contaminants from the previous electroless cobalt-alloy deposition.

[45] Figure 6B shows an embodiment of a schematic diagram of an integrated system 650 that allows minimal exposure of substrate surface to oxygen at critical steps after barrier and copper surface preparation. In addition, since it is an integrated system, the substrate is transferred from one process station immediately to the next process station, which limits the duration that clean copper surface is exposed to low levels of oxygen. The integrated system 650 can be used to process substrate(s) through the entire process sequence of flow 600 of Figure 6A.

[46] The integrated system 650 has 3 substrate transfer modules 660, 670, and 680. Transfer modules 660, 670 and 680 are equipped with robots to move substrate 655 from one process area to another process area. The process area could be a substrate cassette, a reactor, or a loadlock. Substrate transfer module 660 is operated under lab ambient. Module 660 interfaces with substrate loaders (or substrate cassettes) 661 to bring the substrate 655 into the integrated system or to return the substrate to one of the cassettes 661.

[47] As described above in process flow 600 of Figure 6A, the substrate 655 is brought to the integrated system 650 to deposit barrier layer, to prepare barrier surface for copper layer deposition. As described in step 601 of process flow 600, top contact surface 125a of contacts 125 is etched to remove native metal oxide. Once the metal oxide is removed, the exposed tungsten surface 125a of Figure 2A needs to be protected from exposure to oxygen. If the removal process is an Ar sputtering process, the Ar sputtering reactor 671 is coupled to the vacuum transfer module 670. If a wet chemical etching process is selected, the reactor should be coupled to the controlled-ambient transfer module 680, not the lab-ambient transfer module 660, to limit the exposure of the clean tungsten surface to oxygen. For a wet process to be integrated in a system with controlled processing and transporting environment, the reactor needs to be integrated with a rinse/dryer to enable dry-in/dry-out process capability. In addition, the system needs to be filled with inert gas to ensure minimal exposure of the substrate to oxygen.

[48] Afterwards, the substrate is deposited with the barrier layer. The barrier layer 130 of Figure 2B can be deposited by a PVD or an ALD process. In one embodiment, the barrier layer 130 is deposited by an ALD process, which is a dry process and is operated at less than

1 Torr. The ALD reactor 672 is coupled to the vacuum transfer module 670. The substrate can undergo an optional hydrogen reduction process to ensure the barrier layer surface is metal-rich for functionalization layer deposition. The hydrogen reduction reactor 674 can be coupled to the vacuum transfer module 670. At this stage, the substrate is ready for chemical-grafting complexing compound functionalization layer deposition. As described above, in one embodiment, this process is a wet process and can be deposited in a chemical-grafting complexing compound deposition chamber 683, coupled to the controlled-ambient transfer module 680. In one embodiment, chamber 683 is integrated a cleaning module (not shown) to clean the substrate 655 after the functionalization layer deposition. In another embodiment, substrate 655 undergoes an optional substrate cleaning step 607, as described in process flow 600. The substrate cleaning process can be a brush clean process, whose reactor 685 can be integrated with the controlled-ambient transfer module 680. After the substrate surface cleaning, substrate 655 is ready for copper seed layer deposition, as described in step 608 of flow 600. In one embodiment, the copper seed layer deposition is performed by an electroless process. The electroless copper plating can be performed in an electroless copper plating reactor 681 to deposit a conformal copper seed layer, as described in step 608 of Figure 6A. As described above, the deposition of the gap fill copper layer at step 609 of Figure 6A can be deposited in the same electroless plating reactor 681 with different chemistry, or in a separate ECP reactor 681'.

[49] Before the substrate leaves the integrated system 650, the substrate can optionally undergoes a surface cleaning process, which can clean residues from the previous copper plating process. The substrate cleaning process can be brush clean process, whose reactor 663 can be integrated with the lab-ambient transfer module 660.

[50] The wet processing systems described in Figure 6B, which are coupled to the controlled-ambient transfer module 680, all need to meet the requirement of dry-in/dry-out to allow system integration. In addition, the systems are filled with one or more inert gases to ensure minimal exposure of the substrate to oxygen.

[51] The process flow 600 described in Figure 6A and system 650 described in Figure 6B can be used to deposit barrier layer and copper for dual damascene structures, as shown in Figures 1A-1D. For dual damascene structures, step 601 in flow 600 is replaced by cleaning top surface of metal line, which is shown as surface 122a of Figure 1A.

[52] While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention. In the claims, elements and/or steps do not imply any particular order of operation, unless explicitly stated in the claims.

CLAIMS

1. A method of preparing a substrate surface of a substrate to deposit a functionalization layer over a metallic barrier layer of a copper interconnect to assist deposition of a copper layer in the copper interconnect in an integrated system in order to improve electromigration performance of the copper interconnect, comprising:

depositing the metallic barrier layer to line the copper interconnect structure in the integrated system, wherein after depositing the metallic barrier layer, the substrate is transferred and processed in controlled environment to prevent the formation of metallic barrier oxide;

depositing the functionalization layer over the metallic layer in the integrated system;
and

depositing the copper layer in the copper interconnect structure in the integrated system after the functionalization layer is deposited over the metallic barrier layer.

2. The method of claim 1, further comprising:

cleaning an exposed surface of a underlying metal to the copper interconnect to remove a surface metal oxide of the exposed surface of the underlying metal in the integrated system before depositing the metallic barrier layer, wherein the underlying metal is part of an underlying interconnect electrically connected to the copper interconnect;

3. The method of claim 1, further comprising:

reducing a surface of the metallic barrier layer to make the surface of the metallic barrier layer metal-rich in the integrated system before depositing the functionalization layer.

4. The method of claim 1, wherein the material of the metallic barrier layer is selected from the group consisting of tantalum nitride (TaN), tantalum (Ta), Ruthenium (Ru), titanium (Ti), tungsten (W), zirconium (Zr), hafnium (Hf), molybdenum (Mo), niobium (Nb), vanadium (V), ruthenium (Ru) and chromium (Cr), and a hybrid combination of these materials.

5. The method of claim 1, wherein the material used for the functionalization layer comprises a complexing group with at least two ends, one end of the complexing group forming a bond with the metallic barrier layer and another end of the complexing group forming a bond with copper.
6. The method of claim 4, wherein the complexing group is selected from the group consisting of decanethiol, octadecanethiol, tetraphenylporphines, diphenyl disulfide, aromatic thioacetate, ruthenium (II) tris(2, 2, prime-bipyridine) thiol, thiophenol, 4, 4 prime-dithiodipyridine, naphthalene disulfide, and bis(2-anthraquiny) disulfide, 3-mercaptopropyl trimethoxysilane, γ -methacryloxypropyl triethoxysilane, perfluorooctanoxylpropyl-dimethyl silane, alkyltrichlorosilane, octadecylsiloxane, octanol, 22-mercapto-1-docosanoic acid, alkanephosphonic acids, octadecanoic acid, diaminododecane, n-phenylpyrrole, and 2,5-dithienylpyrrol triad.
7. The method of claim 3, wherein reducing the surface of the metallic barrier layer is performed by using a hydrogen-containing plasma.
8. The method of claim 1, wherein the copper interconnect include a metal line over a via and the underlying interconnect include a metal line.
9. The method of claim 1, wherein the copper interconnect include a metal line and the underlying interconnect include a contact.
10. The method of claim 2, wherein cleaning the exposed surface of the surface metal oxide is accomplished by using one of an Ar sputtering process or a plasma process using a fluorine-containing gas.
11. The method of claim 10, wherein the fluorine-containing gas is NF_3 , CF_4 , or a combination of both.

12. The method of claim 1, wherein depositing the metallic barrier layer further comprising:

depositing a first metallic barrier layer; and

depositing a second metallic barrier layer.

13. The method of claim 12, wherein the first metallic barrier layer is deposited by an atomic layer deposition (ALD) process and the second metallic barrier layer is deposited by a physical vapor deposition (PVD) process.

14. The method of claim 12, wherein the first metallic barrier layer is deposited by an ALD process and the second metallic barrier layer is deposited by an ALD process.

15. The method of claim 1, further comprising:

cleaning a surface of the functionalization layer in the integrated system before depositing the copper layer.

16. The method of claim 1, wherein selectively the thin copper seed layer is deposited by an electroless process.

17. The method of claim 1, wherein the gap-fill copper layer is deposited by an electrochemical plating (ECP) process.

18. The method of claim 1, wherein the copper layer replaces the functionalization layer and deposits directly on the metallic barrier layer.

19. An integrated system for processing a substrate in controlled environment to enable deposition of a functionalization layer over a metallic barrier layer of a copper interconnect to improve electromigration performance of the copper interconnect, comprising:

a lab-ambient transfer chamber capable of transferring the substrate from a substrate cassette coupled to the lab-ambient transfer chamber into the integrated system;

a vacuum transfer chamber operated under vacuum at a pressure less than 1 Torr;

a vacuum process module for depositing the metallic barrier layer, wherein the vacuum process module for depositing the metallic barrier layer is coupled to the vacuum transfer chamber, and is operated under vacuum at a pressure less than 1 Torr;

a controlled-ambient transfer chamber filled with an inert gas selected from a group of inert gases; and

a deposition process module used to deposit the functionalization layer on the surface of the metallic barrier layer, wherein the deposition process module used to deposit the functionalization layer is coupled to the controlled-ambient transfer chamber.

20. The integrated system of claim 19, further comprising:

an electroless copper deposition process module used to deposit a thin layer of copper seed layer in the copper interconnect after the functionalization layer is deposited on the surface of the metallic barrier layer, wherein the electroless copper deposition process module is coupled to the controlled-ambient transfer chamber.

21. The integrated system of claim 19, further comprising:

a vacuum process module for cleaning an exposed surface of a metal oxide of a underlying metal, wherein the underlying metal is part of a underlying interconnect, the copper interconnect is electrically connected to the underlying interconnect, and the vacuum process module for cleaning is coupled to the vacuum transfer chamber, and is operated under vacuum at a pressure less than 1 Torr.

22. The integrated system of claim 19, further comprising:

a hydrogen-containing reduction process module used to reduce metal oxide or metal nitride on a surface of the metallic barrier to make the surface metal-rich before the functionalization layer is deposited on the surface of the metallic barrier layer, wherein the hydrogen-containing reduction process module is coupled to the vacuum transfer chamber, the hydrogen-containing reduction process module is operated under vacuum at a pressure less than 1 Torr.

23. The integrated system of claim 20, wherein the electroless copper deposition process module is also used to deposit a gap-fill copper layer over the thin copper seed layer.

24. The integrated system of claim 20, further comprising:

an electroless copper deposition process module to deposit a gap-fill copper layer over the thin copper seed layer.

25. The integrated system of claim 19, further comprising:

a substrate cleaning process module used to clean the substrate surface after depositing the functionalization layer over the metallic barrier layer, wherein the substrate cleaning process module is coupled to the controlled-ambient transfer module.

26. The integrated system of claim 19, further comprising:

a first loadlock coupled to the vacuum transfer chamber and the controlled-ambient transfer chamber, wherein the first loadlock assists the substrate to be transferred between the vacuum transfer chamber and the controlled-ambient transfer chamber, the first loadlock being configured to be operated under vacuum at pressure less than 1 Torr or to be filled with an inert gas selected from a group of inert gases; and

a second loadlock coupled to the vacuum transfer chamber and the lab-ambient transfer chamber, wherein the second loadlock assists the substrate to be transferred between the vacuum transfer chamber and the lab-ambient transfer chamber, the second loadlock being configured to be operated under vacuum at pressure less than 1 Torr or at lab ambient or to be filled with an inert gas selected from a group of inert gases.

27. The integrated system of claim 19, wherein the vacuum transfer chamber and the at least one vacuum process module coupled to the vacuum transfer chamber are operated at a pressure less than 1 Torr to control the exposure of the substrate to oxygen.

28. The integrated system of claim 19, wherein the controlled-ambient transfer chamber and each one the at least one process module coupled to the controlled-ambient transfer chamber are filled with one or more inert gases selected from the group of inert gases to control the exposure of the substrate to oxygen.

29. The integrated system of claim 19, wherein substrate is transferred and processed in the integrated system to limit a duration the substrate is exposed to oxygen.

30. The method of claim 29, wherein limiting the exposure of the substrate surface to oxygen enables the functionalization layer being deposited on the surface of the metallic barrier layer.

31. The integrated system of claim 19, wherein the at least one process module coupled to the controlled-ambient transfer module enables a dry-in/dry-out processing of the substrate, wherein the substrate goes in and comes out the at least one process module in a dry state.