CLAIMS

What is claimed is:

1. A microelectronic package comprising:

a substrate;

a die embedded within the substrate, the die having a front side and an opposing back side and further having at least one through-silicon-via therein;

a plurality of build-up layers adjacent to and built up over the front side of the die; and

a power plane adjacent to and in physical contact with the back side of the die.

2. The microelectronic package of claim 1 wherein:

the power plane comprises copper.

3. The microelectronic package of claim 1 further comprising:

a passive component attached to the power plane; and

a protective layer over the power plane.

4. The microelectronic package of claim 1 wherein:

the power plane has a recess therein; and

the die is at least partially located within the recess.

5. The microelectronic package of claim 1 wherein:

the die has a die perimeter;

an extension of the die perimeter through the build-up layers defines a die area; and

the build-up layers contain a first plurality of vias outside the die area and a second plurality of vias inside the die area.

6. The microelectronic package of claim 5 wherein:

the first plurality of vias electrically connect the power plane and the substrate to each other; and

the second plurality of vias electrically connect the die and the substrate to each other.

7. A microelectronic package comprising:

a substrate;

a first die and a second die, both of which are embedded in the substrate, both of which have a front side and an opposing back side, and both of which have at least one through-silicon-via therein;

a plurality of build-up layers adjacent to and built up over the front sides of the first and second dies; and

an electrically conductive structure adjacent to and in physical contact with the back sides of the first and second dies.

8. The microelectronic package of claim 7 wherein:

the electrically conductive structure comprises:

an interconnect that electrically connects the back sides of the first and second dies to each other; and

a die connection pad.

9. The microelectronic package of claim 8 wherein:

the first die has a first die perimeter and the second die has a second die perimeter;

an extension of the first and second die perimeters through the build-up layers defines a die area; and

the build-up layers contain a first plurality of vias outside the die area and a second plurality of vias inside the die area.

10. The microelectronic package of claim 9 wherein:

the first plurality of vias electrically connect the die connection pad and the substrate to each other; and

the second plurality of vias electrically connect the first and second dies and the substrate to each other.

11. The microelectronic package of claim 7 wherein:

the electrically conductive structure comprises copper.

12. The microelectronic package of claim 7 further comprising:

a protective layer over the electrically conductive structure.

13. The microelectronic package of claim 7 wherein:

the electrically conductive structure has a recess therein; and

the first die and the second die are at least partially located within the recess.

14. A method of manufacturing a microelectronic package, the method comprising:

providing an electrically conductive carrier;

providing a die having a front side, an opposing back side, and at least one through-silicon-via therein;

attaching the back side of the die to the electrically conductive carrier;

forming a plurality of build-up layers over the front side of the die, the build-up layers and the electrically conductive carrier forming part of a substrate of the microelectronic package; and

patterning the electrically conductive carrier in order to form an electrically conductive component of the microelectronic package.

15. The method of claim 14 wherein:

the electrically conductive component is a power plane.

16. The method of claim 15 further comprising:

electrically connecting the power plane to a power source; and

electrically connecting the substrate to the power source.

17. The method of claim 14 wherein:

the microelectronic package further comprises a second die; and

the electrically conductive component is an electrical connection between the die and the second die.

18. The method of claim 14 wherein:

the electrically conductive carrier comprises copper.

19. The method of claim 14 further comprising:

forming a plurality of connection pads adjacent to the electrically conductive component.

20. The method of claim 14 wherein:

providing the electrically conductive carrier comprises providing a copper foil attached to a sacrificial core;

the method further comprises separating the copper foil from the sacrificial core after the build-up layers are completed; and

patterning the electrically conductive carrier in order to form the electrically conductive component of the microelectronic package comprises patterning the copper foil.

CLAIMS

What is claimed is:

1. A microelectronic package comprising:

a substrate;

a first die and a second die, both of which are embedded in the substrate, both of which have a front side and an opposing back side, and both of which have at least one through-silicon-via therein;

a plurality of build-up layers adjacent to and built up over the front sides of the first and second dies; and

an electrically conductive structure adjacent to and in physical contact with the back sides of the first and second dies.

2. The microelectronic package of claim 1 wherein: the electrically conductive structure comprises:

an interconnect that electrically connects the back sides of the first and second dies to each other; and a die connection pad.

3. The microelectronic package of claim 2 wherein:

the first die has a first die perimeter and the second die has a second die perimeter;

an extension of the first and second die perimeters through the build-up layers defines a die area; and

the build-up layers contain a first plurality of vias outside the die area and a second plurality of vias inside the die area.

4. The microelectronic package of claim 3 wherein:

the first plurality of vias electrically connect the die connection pad and the substrate to each other; and

the second plurality of vias electrically connect the first and second dies and the substrate to each other.

5. The microelectronic package of claim 1 wherein: the electrically conductive structure comprises

copper.

6. The microelectronic package of claim 1 further comprising:

a protective layer over the electrically conductive structure.

7. The microelectronic package of claim 1 wherein:

the electrically conductive structure has a recess therein; and

the first die and the second die are at least partially located within the recess.

8. A method of manufacturing a microelectronic package, the method comprising:

providing an electrically conductive carrier;

providing a first die and a second die, the first die having a front side, an opposing back side, and at least one through-silicon-via therein;

attaching the back side of the first die to the electrically conductive carrier;

forming a plurality of build-up layers over the front side of the first die, the build-up layers and the electrically conductive carrier forming part of a substrate of the microelectronic package; and

patterning the electrically conductive carrier in order to form an electrically conductive component of the microelectronic package, the electrically conductive component being an electrical connection between the first die and the second die.

9. The method of claim 8 wherein:

the electrically conductive component is a power plane.

10. The method of claim 9 further comprising:

electrically connecting the power plane to a power source; and

electrically connecting the substrate to the power source.

11. The method of claim 8 wherein:

the electrically conductive carrier comprises copper.

12. The method of claim 8 further comprising:

forming a plurality of connection pads adjacent to the electrically conductive component.

13. The method of claim 8 wherein:

providing the electrically conductive carrier comprises providing a copper foil attached to a sacrificial core;

the method further comprises separating the copper foil from the sacrificial core after the build-up layers are completed; and

patterning the electrically conductive carrier in order to form the electrically conductive component of the microelectronic package comprises patterning the copper foil.