Surface Treatment of Metal Interconnect Lines

TECHNICAL FIELD

[0001] The present invention relates generally to the use of a capping layer over conductors formed by a Damascene etch scheme, and more particularly to the use of forming an alloy layer comprised of metal from the metal conductors deposited by the Damascene process and a second metal formed over the conductors or leads.

BACKGROUND

[0002] As is well known by those skilled in the art, a continuing goal in manufacturing and production of semiconductors is a reduction in size of components and circuits with the concurrent result of an increase in the number of circuits and/or circuit elements such as transistors, capacitors, etc., on a single semiconductor device. This relentless and successful reduction in size of the circuit elements has also required reduction in the size of the conductive lines connecting devices and circuits. However, as the conducting lines are designed to be smaller and smaller, the resistance of the interconnects increases. Further, as the number of dielectric layers increases, the capacitive coupling between lines on the same level and adjacent level increases.

[0003] In the past, aluminum was used as the metal interconnect lines and silicon oxide as the dielectric. However, newer manufacturing techniques now favor copper as the metal for interconnect lines and various low K materials (organic and inorganic) are favored as the dielectric material. Not surprisingly, these material changes have required changes in the processing methods. In particular, because of the difficulty of etching copper without also causing unacceptable damage to the dielectric material, the technique of forming the metal

interconnect lines has experienced significant changes. Namely, whereas aluminum interconnects could be formed by depositing a layer of aluminum and then using photoresist, lithography, and etching to leave a desired pattern of aluminum lines, the formation of copper interconnect lines are typically formed by a process now commonly referred to as a Damascene process. The Damascene process is almost the reverse of etching, and simply stated a trench, canal or via is cut, etched or otherwise formed in the underlying dielectric and is then filled with metal (i.e., copper).

[0004] Unfortunately, although copper has the advantages discussed above, it readily diffuses into dielectric material used in the manufacture of semiconductor devices, and it diffuses especially easily into silicon dioxide. Diffusion of copper into the dielectric materials of a semiconductor deice can cause serious reliability problems including electrical shorts. Therefore, it is typical to form a barrier layer between the copper used for conductors and leads and the dielectric material of a semiconductor device. Typical barrier layers may be formed of Ta (tantalum), TaN (tantalum nitride), Ti (titanium), TiN (titanium nitride) and various combinations of these metals as well as other metal. The barrier layer is typically formed on the bottom and sidewalls of the trenches and vias of the copper interconnects to prevent the copper from diffusing into the surrounding silicon dioxide as other dielectric material. A layer of silicon nitride is then typically deposited as a cover layer over the complete structure including the conductor areas and the dielectric layer before another layer or level of dielectric structure is deposited.

[0005] Unfortunately, silicon nitride adheres poorly to copper and may peel away thereby creating poor interface properties including a path for copper to diffuse into the subsequent or

cover layer of dielectric material. The same path may also allow moisture and contaminants to diffuse from outside into the copper so as to form porous copper oxide.

[0006] Various ones of the above-mentioned problems have been addressed by the prior art, but none of the known prior art provides a solution to all of the problems in the simple and elegant method provided by the present invention. For example, U.S. Patent No. 5,380,546, entitled "Multilevel Metallization Process for Electronic Components" and issued to Krishnan, *et al.*, teaches the use of tungsten as both a barrier layer and a capping layer, but does not teach the unique method of forming an alloy as taught by the present invention. U.S. Patent No. 6,130,157, entitled "Method to Form an Encapsulation Layer Over Copper Interconnects" issued to Liu, *et al.*, teaches the use of several metals as a barrier layer and "treats" a tungsten capping layer with a nitrogen plasma, but does not teach nickel as the capping layer or simply heating to form an alloy as taught by the method of the present invention. U.S. Patent No. 6,261,950, entitled "Self-Aligned Metal Caps for Interlevel Metal Connections" issued to Tobben, *et al.*, does not teach the use of a barrier layer and teaches a first embodiment that selectively deposits a capping layer, but does not teach forming an alloy. The '950 patent also teaches a second embodiment that does not selectively deposit a second metal but does include a heat treatment although at a greater temperature than the present invention. A paper by T. Saito, *et al.*, in proceedings of the IITC in 2001 at pages 15-17 teaches a self aligned metal capping process for Copper damascene interconnect. A Tungsten capping layer is selectively formed on the Cu interconnect using the preferential deposition phenomenon of W-CVD assisted by pre and post treatment. This technology is applied to 0.2µm bipolar-CMOS LSI with multilevel Cu interconnects, and then yield, reliability and operation speed are evaluated.

SUMMARY OF THE INVENTION

[0007] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by the present invention which discloses methods and apparatus for forming a semiconductor structure comprising a first layer comprised of conductive regions such as copper or other metal interconnect lines and non-conductive regions such as a silicon dioxide dielectric or other non-conductive materials. A layer of a second metal that is different from the metal of the conductive regions is formed or deposited on the conductive region such as by a electrochemical deposition process including electroless plating. The electroless plating may be carried out by placing the substrate with the conductive and non-conductive region into a electroless plating chemical bath comprised of a metal ion chelate (such as a Ni (nickel ion chelate), a reduction agent such as sodium hypophosphite or Hydrazine and, if necessary, one or more agents or additives such as the accelerator sodium adipate, etc. The substrate including the layer of a first metal formed as the conductive region and the second metal of the cover layer interact to form an alloy such as for example, a copper/nickel (Cu/Ni) alloy. The surface of the second Cu/Ni layer is then cleaned by one or more various cleaning processes well known by those skilled in the art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0009] FIG. 1 is a prior art illustration of a semiconductor structure comprising a substrate covered by conductive regions and non-conductive regions;

[0010] FIG. 2A is an enlarged view of conductive regions of FIG. 1;

[0011] FIG. 2B illustrates the view of FIG. 1 after a second metal has been formed over the conductive regions according to the teachings of this invention;

[0012] FIG. 2C illustrates the structure of FIG. 2B after heating the semiconductive structure so as to cause the metal of the conductive regions and the second metal to react with each other to form an alloy; and

[0013] FIG. 2D illustrates an alternate embodiment of FIG. 2C wherein the thickness of the second metal layer was greater than the depth of the copper ion migration such that there is an alloy layer and a top layer of the second metal.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0014] Referring now to FIG. 1, there is shown a typical semiconductor structure including a substrate 10 having a first layer of non-conductive regions 12 and conductive or interconnect regions 14. It should be appreciated that the term substrate 10 as used herein may simply be a silicon wafer or alternately may represent one or more layers of various semiconductor devices including interconnecting metalization layers. Thus, the term substrate is intended to be broadly interpreted. For example, typically the substrate 10 may be comprised of a dielectric layer similar to the non-conductive regions 12 of FIG. 1.

[0015] As is well known by those skilled in the art, the use of the Damascene process and the use of copper as the interconnecting layers has created new problems while at the same time solving other problems. For example, when the conducting or interconnecting lines are made of copper, the copper may diffuse into the surrounding non-conductive or substrate areas if steps are not taken to prevent such diffusion. Thus, as shown in FIG. 1 there is also included a barrier layer 16, which stops or hinders the diffusion of the copper ions from the copper interconnecting strip 14 into the surrounding non-conductive portions or regions 12 and the substrate 10. Suitable barrier layers are well known in the art and include, for example only, Ta (tantalum), TaN (tantalum nitride), Ti (titanium) and TiN (titanium nitride) and various combinations of these and other materials. Thus, when this barrier layer 16 is provided, diffusion of the copper into the surrounding materials is slowed if not substantially eliminated. Further, it is typical to include a cover layer over the non-conductive regions 12 and the conductive regions 14 of a material such as silicon nitride if still another layer of semiconductor devices is to be formed over the first layer 12 and 14. Unfortunately, as was discussed above, the silicon nitride does not adhere well to the copper interconnect line which will typically have been subjected to CMP.

Further, the conductive layer such as a layer of copper may include rough areas with pockets such as pocket 18 and/or dish areas such as dish area 20. Thus, because of the poor adhesion qualities between the copper and the protective layer of silicon nitride, it is not uncommon for serious reliability problems to occur. For example, the layer of silicon nitride (not shown) may peel away leaving no barrier between the copper and the subsequent dielectric layer. Of course as will be appreciated by those skilled in the art, when the barrier of silicon nitride is absent, the copper ions will readily diffuse into the cover layer of a dielectric thereby often causing electrical shorts.

[0016] Referring now to FIG. 2A, there is illustrated an enlarged view of the conductive region or copper interconnect line 14 prior to the processes of the present invention. Therefore, according to the invention a second metal or layer of metal material is deposited over the metal interconnect or copper line 14 such as by electrochemical depositing a metal capping layer which will adhere only to the conductive regions or copper interconnect lines. To form the second layer of metal which adheres to the conductive regions or copper interconnect lines, an electroless plating process, such as ECD (Electroless Chemical Deposition) may be used which includes providing a solution of $NiCH_{2,}GH_2O$ or $NiSO_{4,}GH_2O$. According to another embodiment, an electrolyte solution or chemical bath may be used which includes a metal ion chelate such as for example a nickel ion chelate in the form of EDTA (elhylenediamine tetra-acetic acid) or a citric acid solution, a reduction agent such as for example Sodium Hypophosphite ($Na(H_2PO_2)\ H_20$) or Hydrazine, and one or more additives. It may be desirable to use several additives for different purposes. For example, sodium adipate may be used as an accelerator, thiourea as a stabilizer, sodium carbonate or ammonia as a pH adjustor and ABS-Na as a brightener. Thus, by using the ECD process or an electrolyte solution for electroless

depositing, a second metal, such as nickel, onto the surface of the copper interconnect lines 14, a second layer 22 of the second metal is formed over the copper interconnect lines 14. The combined semiconductor structure of the substrate, the layer of non-conductive region (or dielectric) and conductive regions (copper interconnect lines), and the second metal capping layer 22 formed of another metal different from copper, such as for example nickel, is then subjected to a heat treatment such as a sintering temperature of between 300° and 400° C. This heat treatment will cause an inter reaction between the two metals such as for example the copper and interconnect lines 14 and the deposited nickel 22 to form an alloy layer 22a of the two metals or Cu/Ni. The resulting alloy layer 22a will have improved adhesion with respect to a subsequent dielectric layer and excellent adhering qualities with respect to the copper interconnect line 14 thereby eliminating the tendency of the silicon nitride to peel and further reducing the reliability problems. Other metals suitable for use as the metal capping layer include Co (cobalt) and Pd (palladium). The structure is then preferably cleaned by a standard post CMP cleaning process.

[0017] If the second metal layer is thick enough, or the heat treatment is of too short a duration, the copper ion migration into the second metal layer, (such as nickel), may not reach the top portions of the layer so that the top portion is comprised substantially of nickel alone without copper ions. In this situation, the combined structure will comprise the copper interconnect lines 14, an alloy layer 22a and a second metal layer 22 such as shown in FIG. 2D.

[0018] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

For example, it will be readily understood by those skilled in the art that dimensions and layer thickness may be varied while remaining within the scope of the present invention.

[0019] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, methods, or steps.

WHAT IS CLAIMED IS:

1. A method of forming a semiconductor structure comprising the steps of:

forming a first layer over a substrate, said first layer having non-conductive regions and conductive regions of a first metal;

electrochemically depositing (ECD) a second layer on said conductive regions of said first layer, said second layer being a second metal different than said first metal; and

heating said first layer and said second layer to form an alloy of said first metal and said second metal.

2. The method of claim 1 further comprising the step of cleaning the exposed surface of said second layer of said structure prior to said heating step.

3. The method of claim 1 further comprising the step of forming a barrier layer between said conductive regions and said non-conductive regions.

4. The method of claim 1 wherein one of the solutions $NiCl_2$, GH_20 and $NiSO_4$, GH_20 is used for said ECD process.

5. The method of claim 1 wherein said first metal is copper.

6. The method of claim 5 wherein said second metal is selected from the group consisting of Ni (nickel),Co (cobalt) and Pd (palladium).

7. The method of claim 1 wherein said second metal is nickel.

8. The method of claim 1 wherein said step of heating comprises the step of heating to a temperature of between about 300ºC and 400ºC.

9. A method of forming a semiconductor structure comprising the steps of:

forming a first layer over a substrate, said first layer having non-conductive regions and conductive regions of a first metal;

electroless plating a second layer on said conductive regions of said first layer, said second layer being a second metal different than said first metal; and

heating said first layer and said second layer to form an alloy of said first metal and said second metal.

10. The method of claim 9 wherein said first metal is copper.

11. The method of claim 10 wherein said second metal is selected from the group consisting of Ni (nickel),Co (cobalt) and Pd (palladium).

12. The method of claim 9 wherein said second metal is nickel.

13. The method of claim 9 wherein said step of electroless plating said second layer on said conductive regions of said first layer comprises the steps of providing a chemical bath of a metal ion chelate and a reduction agent.

14. The method of claim 13 wherein said metal ion chelate comprises a nickel ion chelate.

15. The method of claim 13 wherein said reduction agent is selected from the group consisting of sodium hypophosphite ($Na(H_2PO_2)$ H_2O) and hydrazine.

16. The method of claim 13 further comprising at least one additive selected from the group consisting of an accelerator (sodium adipate), a stabilizer (thiourea), a pH adjuster (sodium carbonate and ammonia), and a brightener (ABS-Na).

17. The method of claim 9 further comprising the step of forming a barrier layer between said conductive regions and said non-conductive regions.

18. The method of claim 9 wherein said step of heating comprises the step of heating to a temperature of between about 300ºC and 400ºC.

19. A method of forming a semiconductor structure comprising the steps of:

forming a first layer having copper conductive regions and non-conductive regions over a substrate;

forming a layer of nickel over said conductive regions;

heating said copper layer and said nickel layer to form an alloy layer of copper and nickel; and

cleaning the exposed surface of said second layer.

20. The method of claim 19 wherein said step of forming said nickel layer on said copper layer comprises the step of using an ECD process for electrochemically depositing said nickel layer over said copper layer.

21. The method of claim 20 wherein one of the solutions $NiCl_2\,GH_2O$ and $NiSO_4\,GH_2O$ is used for said ECD process.

22. The method of claim 19 wherein said step of forming said layer of nickel comprises the step of electroless plating nickel on said conductive regions.

23. The method of claim 22 wherein said step of an electroless plating process comprising the step of providing a chemical bath of a nickel ion chelate and a reduction agent.

24. The method of claim 23 wherein said reduction agent is selected from the group consisting of sodium hypophosphite (Na (H_2PO_2) H_2O) and hydrazine.

25. The method of claim 23 further comprising at least one additive selected from the group consisting of an accelerator (sodium adipate), a stabilizer (thiourea), a pH adjuster (sodium carbonate and ammonia), and a brightener (ABS-Na).

26. A semiconductor structure comprising:

a substrate;

a first layer formed on said substrate, said first layer defining at least one conductive region formed of a first metal and at least one non-conductive region; and

a top layer over said at least one conductive region, said top layer comprising an alloy layer formed from a layer of a second metal covering said conductive region and ions of said first metal which have migrated from said conductive region.

27. The semiconductor structure of claim 26 wherein said top layer further comprises a surface position of said second metal beyond the reach of said migrating ions.

28. The semiconductor structures of claim 26 wherein said layer of said second metal is a layer of ECD (electrochemically deposited) metal.

29. The semiconductor structures of claim 26 wherein said layer of said second metal is a layer of electroless plated metal.

30. The semiconductor structures of claim 26 wherein said substrate comprises at least one layer of semiconductor devices.

31. The semiconductor structure of claim 28 wherein migration of ions of said first metal into said second metal of said top layer occurs when said structure is heated to a temperature of less than 400ºC.

32. The semiconductor structure of claim 26 wherein said first metal is copper.

33. The semiconductor structure of claim 32 wherein said second metal is selected from the group consisting of Co (cobalt), Pd (palladium) and Ni (nickel).

34. The semiconductor structure of claim 26 wherein said second metal is selected from the group consisting of Co (cobalt), Pd (palladium) and Ni (nickel).

35. The semiconductor structure of claim 26 further comprising a barrier layer formed between said conductive regions and said non-conductive regions.