ABSTRACT

A METHOD TO AVOID COPPER CONTAMINATION ON THE SIDEWALL OF A VIA OR A DUAL DAMASCENE STRUCTURE

A new method to prevent copper contamination of the intermetal dielectric layer during via or dual damascene etching by forming a capping layer over the first copper metallization is described. A first copper metallization is formed in a dielectric layer overlying a semiconductor substrate wherein a barrier metal layer is formed underlying the first copper metallization and overlying the dielectric layer. The first copper metallization is planarized, then etched to form a recess below the surface of the dielectric layer. A conductive capping layer is deposited overlying the first copper metallization within the recess and overlying the dielectric layer. The conductive capping layer is removed except over the first copper metallization within the recess using one of several methods. An intermetal dielectric layer is deposited overlying the dielectric layer and the conductive capping layer overlying the first copper metallization. A via or dual damascene opening is etched through the intermetal dielectric layer to the conductive capping layer wherein the conductive capping layer prevents copper contamination of the intermetal dielectric layer during etching. The via or dual damascene opening is filled with a metal layer to complete electrical connections in the fabrication of an integrated circuit device.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)