Although this approach delivers good results in terms of aliasing robustness, it has some disadvantages. First, the MDST coefficients are estimated and their accuracy is defined by the amount of computational complexity. Second, the transform chain R2C-C2R produces still delay.

[1] H. S. Malvar, “A modulated complex lapped transform and its applications to audio processing”, in Proc. IEEE Int. Conf. on Acoustics, Speech, and Signal Processing (ICASSP), Phoenix, March 1999.

[2] Kuech, F.; Edler, B., “Aliasing Reduction for Modified Discrete Cosine Transform Domain Filtering and its Application to Speech Enhancement”, in IEEE Workshop on Applications of Signal Processing to Audio and Acoustics, 21-24 Oct. 2007.

[3] Edler, B., “Aliasing Reduction for Gain Control with Critically Sampled Filter Banks”, in First International Conference on Communications and Electronics, ICCE '06, 10-11 Oct. 2006.

[4] E. Larsen and R. M. Aarts. Audio Bandwidth Extension - Application to psychoacoustics, Signal Processing and Loudspeaker Design. John Wiley & Sons, Ltd, 2004.

[5] M. Dietz, L. Liljeryd, K. Kjörling and O. Kunz, “Spectral Band Replication, a novel approach in audio coding,” in 112th AES Convention, Munich, May 2002.

[6] P. Ekstrand, “Bandwidth Extension of Audio Signals by Spectral Band Replication”, in Proceedings of 1st IEEE Benelux Workshop on MPCA, Leuven, November 2002

It is an object of the present invention to provide an improved concept for processing an audio signal.

This object is achieved by an apparatus for processing an audio signal of claim 1, a method of processing an audio signal of claim 12 or a computer program of claim 13.

In an aspect of the present invention, an apparatus for processing an audio signal comprising a sequence of blocks of spectral values comprises a processor for processing the sequence of blocks of spectral values using at least one modification value for a first block to obtain an aliasing reduced or aliasing free first result signal in an overlap range and using at least one second different modification value from a second block of the sequence of blocks of spectral values to obtain aliasing reduced or aliasing free second result signal in the overlap range. Then, both signals in the overlap range, both of which

Claims

1. Apparatus for processing an audio signal comprising a sequence of blocks of spectral values, comprising:

a processor for calculating an aliasing-affected signal using at least one first modification value for a first block of the sequence of blocks and using at least one different second modification value for a second block of the sequence of blocks and for estimating an aliasing-error signal representing an aliasing-error in the aliasing-affected signal; and

a combiner for combining the aliasing-affected signal and the aliasing-error signal such that a processed signal obtained by the combining is an aliasing-reduced or aliasing-free signal,

wherein the processor comprises:

a modifier for modifying the first block using the at least one first modification value to obtain a first modified block, for modifying the second block using the at least one second modification value to obtain a second modified block, and for modifying the first block and the second block using the at least one first or the at least one second modification value to obtain a third modified block and a fourth modified block;

a spectrum-time converter for converting the first to fourth modified blocks into time domain representations; and

an overlap-adder for overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and for overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combiner comprises an aliasing signal manipulator for manipulating the aliasing signal, and

wherein the combiner comprises an adder for adding a manipulated aliasing-error signal and the aliasing-affected signal, or

wherein the processor comprises:

a gain modifier for modifying the first block using the at least one first modification value to obtain a first modified block, for modifying the second block using the at least one second modification value to obtain a second modified block, for modifying the second block using a combination between the at least one first modification value and the at least one second modification value to obtain a third modified block, and for modifying the first block using the difference of the at least one first modification value and the at least one second modification value to obtain a fourth modified block;

a spectrum-time converter for converting the first to fourth modified blocks into time domain representations; and

an overlap-adder-adding for overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and for overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combiner comprises an aliasing signal manipulator for manipulating the aliasing error signal, and

wherein the combiner comprises an adder or a subtractor for adding or subtracting a manipulated aliasing-error signal and the aliasing-affected signal, or

wherein the processor comprises:

a gain modifier for modifying the first block using the at least one first modification value, wherein the first block is generated using a patching function associated with the first block to obtain a first modified block, for modifying the second block using the at least one second modification value, wherein the second block is generated by a patching operation associated with the second

block to obtain a second modified block, for modifying the first block using the at least one second modification value, wherein the first block has been obtained by using the patching operation associated with the second block to obtain a first intermediate third modified block, for modifying the first block obtained by having applied the patching operation associated with the first block using the at least one first modified value to obtain a second third intermediate modified block, for combining the first and the second third intermediate modified blocks to obtain the third modified block, for modifying the second block obtained by having applied the patching operation associated with the second block using the at least one second modification value to obtain a first intermediate fourth modified block, for modifying the second block having obtained by applying the patching operation associated with the first block using the at least one first modification value to obtain a second intermediate fourth modified block and for combining the first and the second fourth intermediate modified blocks to obtain the fourth modified block;

a spectrum-time converter for converting the first to fourth modified blocks into time domain representations; and

an overlap-adder-adder for overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and for overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combiner comprises an aliasing signal manipulator for manipulating the aliasing-error signal, and

wherein the combiner comprises an adder for adding a manipulated aliasing-error signal and the aliasing-affected signal.

2. Apparatus of claim 1,

wherein the aliasing signal manipulator comprises at least one of the following elements:

a windower for applying a window function, and a time reverser for applying a time reversal operation.

3. Apparatus of one of the preceding claims,

wherein the combiner is configured to add the aliasing-error signal to the aliasing-affected signal, when a difference between the at least first modification value and the at least one second modification value is calculated by subtracting the at least one first modification value from the at least one second modification value, and wherein the combiner is configured to add the aliasing-error signal to the aliasing-affected signal, when, for the calculation of the difference, the at least one second modification value is subtracted from the at least one first modification value.

4. Apparatus of one of the preceding claims,

wherein the processor is configured to perform an inverse modified discrete cosine transform operation in performing a spectrum-time conversion.

5. Apparatus of one the preceding claims,

wherein the processor is configured to perform an overlap-add processing operation in calculating the first and second result signals in the overlap range, and

wherein the combiner is configured to combine the first and second result signals in a combining range, wherein the combining range is identical to the overlap range.

6. Apparatus of one of the preceding claims,

wherein the processor is configured for applying a bandwidth filling operation having a patching function to patch spectral values from a source range to a target range, and

wherein the processor is configured for applying the patching function in calculating the first and second result signals.

7. Apparatus of one of the preceding claims,

a patcher for generating the first block in a bandwidth filling range using spectral values from a different frequency range in accordance with a patching function for the first block, and

for generating the second block in a bandwidth filling range having spectral values for a different frequency region in accordance with a patching function associated with the second block.

8. Apparatus of one of the preceding claims,

wherein the processor is configured to perform a multiplication operation to the first and second blocks using the gain functions as modification values.

9. Apparatus of one of the preceding claims,

wherein the processor is configured to apply a spectral-time conversion operation having a spectrum-time transform part and a synthesis window part applied to an output of the spectrum-time transform part.

10. Apparatus of one of the preceding claims,

wherein the processor is configured to operate using modification values varying over time and frequency.

11. Apparatus of one of the preceding claims, wherein the processor is configured for performing lapped transforms having an overlapping range, and wherein the processor is configured for only performing operations influencing values in the overlapping range and for not performing operations not influencing values in the overlapping range.

12. Method for processing an audio signal comprising a sequence of blocks of spectral values, comprising:

calculating an aliasing-affected signal using at least one first modification value for a first block of the sequence of blocks and using at least one different second modification value for a second block of the sequence of blocks and estimating an aliasing-error signal representing an aliasing-error in the aliasing-affected signal; and

combining the aliasing-affected signal and the aliasing-error signal such that a processed signal obtained by the combining is an aliasing-reduced or aliasing-free signal,

wherein the calculating comprises:

modifying the first block using the at least one first modification value to obtain a first modified block, modifying the second block using the at least one second modification value to obtain a second modified block, and modifying the first block and the second block using the at least one first or the at least one second modification value to obtain a third modified block and a fourth modified block;

converting the first to fourth modified blocks into time domain representations; and

overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combining comprises manipulating the aliasing error signal, and

wherein the combining comprises adding a manipulated aliasing-error signal and the aliasing-affected signal, or

wherein the calculating comprises:

modifying the first block using the at least one first modification value to obtain a first modified block, modifying the second block using the at least one second

modification value to obtain a second modified block, modifying the second block using a combination between the at least one first modification value and the at least one second modification value to obtain a third modified block, and modifying the first block using the difference of the at least one first modification value and the at least one second modification value to obtain a fourth modified block;

converting the first to fourth modified blocks into time domain representations; and

overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combining comprises manipulating the aliasing error signal, and

wherein the combining comprises adding or subtracting a manipulated aliasing-error signal and the aliasing-affected signal, or

wherein the calculating comprises:

modifying the first block using the at least one first modification value, wherein the first block is generated using a patching function associated with the first block to obtain a first modified block, modifying the second block using the at least one second modification value, wherein the second block is generated by a patching operation associated with the second block to obtain a second modified block, modifying the first block using the at least one second modification value, wherein the first block has been obtained by using the patching operation associated with the second block to obtain a first intermediate third modified block, modifying the first block obtained by having applied the patching operation associated with the first block using the at least one first modified value to obtain a second third intermediate modified block, combining the first and the second third intermediate modified blocks to obtain the third modified block, modifying the second block obtained by having applied the patching operation associated with the second block using the at

least one second modification value to obtain a first intermediate fourth modified block, modifying the second block having obtained by applying the patching operation associated with the first block using the at least one first modification value to obtain a second intermediate fourth modified block and combining the first and the second fourth intermediate modified blocks to obtain the fourth modified block;

converting the first to fourth modified blocks into time domain representations; and

overlap-adding the time domain representations of the first and second modified blocks to obtain the aliasing-affected signal and overlap-adding the time domain representations of the third and fourth blocks to obtain the aliasing-error signal; and

wherein the combining comprises manipulating the aliasing-error signal, and

wherein the combining comprises adding a manipulated aliasing-error signal and the aliasing-affected signal.

13. Computer program for performing, when running on a computer or a processor, the method of claim 12.