GROWN NANOFIN TRANSISTORS

Cross Reference To Related Applications

Benefit of priority is hereby claimed to "Nanowire Transistor With Surrounding Gate," U.S. Application Serial No. 11/397,527, filed on April 4, 2006; "Etched Nanofin Transistors," U.S. Application Serial No. 11/397,358, filed on April 4, 2006; "DRAM With Nanofin Transistors," U.S. Application Serial No. 11/397,413, filed on April 4, 2006; and "Tunneling Transistor With Sublithographic Channel," U.S. Application Serial No. 11/397,406, filed on April 4, 2006, which applications are herein incorporated by reference.

Technical Field

This disclosure relates generally to semiconductor devices, and more particularly, to nanofin transistors.

Background

The semiconductor industry has a market driven need to reduce the size of devices, such as transistors, and increase the device density on a substrate. Some product goals include lower power consumption, higher performance, and smaller sizes. FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k. The continuous scaling of MOSFET technology to the deep sub-micron region where channel lengths are less than 0.1 micron (100 nm or 1000 Å) causes significant problems in the conventional transistor structures. For example, junction depths should be much less than the channel length. Thus, with reference to the transistor 100 illustrated in FIG. 1, the junctions depths 101 should be on the order of a few hundred Angstroms for channels lengths 102 that are approximately 1000 Å long. Such shallow junctions are difficult to form by conventional implantation and diffusion techniques. Extremely high levels of channel doping are required to suppress short-channel effects such as drain induced barrier lowering, threshold

voltage roll off, and sub-threshold conduction. Sub-threshold conduction is particularly problematic in DRAM technology as it reduces the charge storage retention time on the capacitor cells. These extremely high doping levels result in increased leakage and reduced carrier mobility. Thus, the expected improved performance attributed to a shorter channel is negated by the lower carrier mobility and higher leakage attributed to the higher doping.

Leakage current is a significant issue in low voltage and lower power battery-operated CMOS circuits and systems, and particularly in DRAM circuits. The threshold voltage magnitudes are small to achieve significant overdrive and reasonable switching speeds. However, as illustrated in FIG. 2, the small threshold results in a relatively large sub-threshold leakage current.

Some proposed designs to address this problem use transistors with ultra-thin bodies, or transistors where the surface space charge region scales as other transistor dimensions scale down. Dual-gated or double-gated transistor structures also have been proposed to scale down transistors. As commonly used in the industry, "dual-gate" refers to a transistor with a front gate and a back gate which can be driven with separate and independent voltages, and "double-gated" refers to structures where both gates are driven when the same potential. An example of a double-gated device structure is the FinFET. "TriGate" structures and surrounding gate structures have also been proposed. In the "TriGate" structure, the gate is on three sides of the channel. In the surrounding gate structure, the gate surrounds or encircles the transistor channel. The surrounding gate structure provides desirable control over the transistor channel, but the structure has been difficult to realize in practice.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, and front and back gates separated from a semiconductor body by gate insulators, and also illustrates an electric field generated by the drain. Some characteristics of the dual-gated and/or double-gated MOSFET are better than the conventional bulk silicon MOSFETs, because compared to a single gate, the two gates better screen the electric field generated by the drain electrode from the source-end of the

channel. The surrounding gate further screens the electric field generated by the drain electrode from the source. Thus, sub-threshold leakage current characteristics are improved, because the sub-threshold current is reduced more quickly as the gate voltage is reduced when the dual-gate and/or double gate MOSFET turns off. FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, or surrounding gates MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

FIGS. 5A-C illustrate a conventional FinFET. FIG. 5A illustrates a top view of the FinFET and FIG. 5B illustrates an end view of the FinFET along line 5B-5B. The illustrated FinFET 503 includes a first source/drain region 504, a second source drain region 505, and a silicon fin 506 extending between the first and second source/drain regions. The silicon fin functions as a transistor body, where the channel between the first and second source/drain regions is horizontal. A gate insulator 507, such as silicon oxide, is formed over the fin, and a gate 508 is formed over the fin after the oxide is formed thereon. The fin of the illustrated conventional FinFET is formed over buried oxide 509. FIG. 5C illustrates a conventional etch technique for fabricating the fin for the FINFET. As illustrated in FIG. 5C, the fin width is defined by photolithography or e-beam lithography and etch. Thus, the fin width is initially a minimum feature size (1F). The width of the fin is subsequently reduced by oxidation or etch, as illustrated by arrows 510.

Summary

Aspects of the present subject matter grow ultrathin fins of semiconductor (e.g. silicon) from amorphous semiconductor (e.g. a-silicon) using solid phase epitaxy (SPE) on a crystalline substrate. The SPE process recrystallizes the amorphous semiconductor, using the crystalline substrate to seed the crystalline growth. The amorphous nanofins are formed with dimensions smaller than lithographic dimensions by a sidewall spacer technique.

The nanofins are used as the body regions of CMOS transistors where both the thickness of the body of the transistor and channel length have dimensions smaller than lithographic dimensions. For example, some embodiments provide ultrathin nanofins with a thickness on the order of 20 nm to 50 nm.

One aspect of the present subject matter relates to a method for forming a transistor. According to an embodiment, a fin of amorphous semiconductor material is formed on a crystalline substrate, and a solid phase epitaxy (SPE) process is performed to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth. The fin has a cross-sectional thickness in at least one direction less than a minimum feature size. The transistor body is formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region. A surrounding gate insulator is formed around the semiconductor pillar, and a surrounding gate is formed around and separated from the semiconductor pillar by the surrounding gate insulator.

In an embodiment for forming a transistor, a silicon nitride layer is formed on a silicon wafer, and a hole is etched in the silicon nitride. The hole extends through the silicon nitride layer to the silicon wafer and is defined by the sides of the silicon nitride layer. Amorphous silicon oxide sidewall spacers are formed on the sides of the silicon nitride that define the hole. The silicon nitride layer is removed, leaving the amorphous silicon oxide sidewall spacers on the silicon wafer. The sidewall spacers are crystallized. The sidewall spacers are masked and etched to form at least one silicon fin from the sidewall spacers. The silicon fin is positioned over a doped region to function as a first source/drain region for the transistor. A surrounding gate insulator is formed around the silicon fin, and a surrounding gate is formed around and separated from the silicon fin by the surrounding gate insulator. A second source/drain region is formed in a top portion of the silicon fin.

An aspect relates to a transistor. A transistor embodiment includes a crystalline substrate, a crystalline semiconductor fin on the substrate, a gate

insulator formed around the fin, and a surrounding gate formed around and separated form the fin by the gate insulator. The fin has a cross-sectional dimension that is less than a minimum feature size. The fin provides a vertically-oriented channel between a lower source/drain region and an upper source/drain region.

These and other aspects, embodiments, advantages, and features will become apparent from the following description of the present subject matter and the referenced drawings.

Brief Description of the Drawings

FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k.

FIG. 2 illustrates sub-threshold leakage in a conventional silicon MOSFET.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, front and back gates separated from a semiconductor body by gate insulators, and an electric field generated by the drain.

FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, and surrounding gate MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

FIGS. 5A-C illustrate a conventional FinFET.

FIGS. 6A-6L illustrate a process for forming a nanofin transistor, according to various embodiments of the present subject matter.

FIG. 7 illustrates a top view of a layout of nanofins for an array of nanofin transistors, according to various embodiments of the present subject matter.

FIG. 8 illustrates a process to fabricate a nanofin transistor, according to various embodiments of the present subject matter.

FIG. 9 illustrates a process to form amorphous semiconductor fins, according to various embodiments of the present subject matter.

FIG. 10 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter.

FIG. 11 illustrates a diagram for an electronic system having nanofin transistors.

FIG. 12 depicts a diagram of an embodiment of a system having a controller and a memory.

Detailed Description

The following detailed description refers to the accompanying drawings which show, by way of illustration, specific aspects and embodiments in which the present subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present subject matter. The various embodiments of the present subject matter are not necessarily mutually exclusive as aspects of one embodiment can be combined with aspects of another embodiment. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present subject matter. In the following description, the terms "wafer" and "substrate" are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art. The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side", "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the

orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Disclosed herein are nanofin transistors, and a fabrication technique in which vertical amorphous silicon nanofins are recrystallized on a substrate to make single crystalline silicon nanofin transistors. Aspects of the present subject matter provide nanofin transistors with vertical channels, where there is a first source/drain region at the bottom of the fin and a second source/drain region at the top of the fin. FIGS. 6A-6L illustrate a process for forming a nanofin transistor, according to various embodiments of the present subject matter.

FIGS. 6A and 6B illustrate a top view and a cross-section view along 6B-6B, respectively, of a semiconductor structure 611 with a silicon nitride layer 612, holes 613 in the silicon nitride layer, and sidewall spacers 614 of amorphous silicon along the walls of the holes. The holes are etched in the silicon nitride layer, and amorphous silicon deposited and directionally etched to leave only on the sidewalls. The holes 613 are etched through the silicon nitride layer 612 to a silicon wafer or substrate 615.

FIGS. 6C and 6D illustrate a top view and a cross-section view along line 6D-6D, respectively, of the structure after the silicon nitride layer is removed. As illustrated, after the silicon nitride layer is removed, the sidewalls 614 are left as standing narrow regions of amorphous silicon. The resulting patterns of standing silicon can be referred to as "racetrack" patterns, as they have a generally elongated rectangular shape. The width of the lines is determined by the thickness of the amorphous silicon rather than masking and lithography. For example, the thickness of the amorphous silicon may be on the order of 20 nm to 50 nm, according to various embodiments. A solid phase epitaxial (SPE) growth process is used to recrystallize the standing narrow regions of amorphous silicon. The SPE growth process includes annealing, or heat treating, the structure to cause the amorphous silicon to crystallize, beginning at the interface with the

silicon substrate 615 which functions as a seed for crystalline growth up through the remaining portions of the standing narrow regions of silicon.

FIG. 6E illustrates a top view of the structure 611, after a mask layer has been applied. The shaded areas are etched, leaving free-standing fins formed of crystalline silicon. FIGS. 6F and 6G illustrate a top view and a cross-section view along line 6G-6G, respectively, of the pattern of free-standing fins 616. A buried doped region 617 functions as a first source/drain region. According to various embodiments, the buried doped region can be patterned to form a conductive line either the row or column direction of the array of fins.

FIG. 6H illustrates a top view of the structure, where the fins have been surrounded by a gate insulator 618 and a gate 619. The gate insulator can be deposited or otherwise formed in various ways. For example, a silicon oxide can be formed on the silicon fin by a thermal oxidation process. The gate can be any gate material, such as polysilicon or metal. The gate material is deposited and directionally etched to leave the gate material only on the sidewalls of the fin structure with the gate insulator. The wiring can be oriented in either the "x-direction" or "y-direction."

FIGS. 6I and 6J illustrate a top view and a cross-section view along line 6J-6J, respectively, of the structure illustrated in FIG. 6H after the structure is backfilled with an insulator 620 and gate wiring 621 is formed in an "x-direction" along the long sides of the fins. Various embodiments backfill the structure with silicon oxide. Trenches are formed in the backfilled insulator to pass along a side of the fins, and gate lines are formed in the trenches. In various embodiments, one gate line passes along one side of the fins, in contact with the surrounding gate of the fin structure. Some embodiments provide a first gate line on a first side of the fin and a second gate line on a second side of the fin. The gate wiring material, such as polysilicon or metal, can be deposited and directionally etched to leave on the sidewalls only. The gate wiring material appropriately contacts the surrounding gates for the fins. In various embodiments, the gate material and gate wiring material are etched to recess the

gate and gate wiring below the tops of the fins. The whole structure can be backfilled with an insulator, such as silicon oxide, and planarized to leave only oxide on the surface. The top of the pillars or fins can be exposed by an etch. A second source/drain region 622 can be implanted in a top portion of the fins, and metal contacts 623 to the drain regions can be made by conventional techniques. The metal wiring can run, for example, in the "x-direction" and the buried source wiring run perpendicular, in the plane of the paper in the illustration.

FIGS. 6K and 6L illustrate a top view and a cross-section view along line 6L-6L, respectively, of the structure after the structure is backfilled with an insulator and gate wiring is formed in an "y-direction" along the short sides of the fins. Trenches are opened up along the side of the fins in the "y-direction." Gate wiring material 621, such as polysilicon or metal, can be deposited and directionally etched to leave on the sidewalls only and contacting the gates on the fins. In various embodiments, the gate material and gate wiring material are etched to recess the gate and gate wiring below the tops of the fins. The whole structure can be backfilled with an insulator 620, such as silicon oxide, and planarized to leave only the backfill insulator on the surface. Contact openings and drain doping regions 622 can then be etched to the top of the pillars and drain regions implanted and metal contacts to the drain regions made by conventional techniques. The metal wiring can run, for example, perpendicular to the plane of the paper in the illustration and the buried source wiring runs in the "x-direction." The buried source/drains are patterned and implanted before deposition of the amorphous silicon. FIG. 6L gives an illustration of one of the completed fin structures with drain/source regions, recessed gates, and source/drain region wiring. These nanofin FET's can have a large W/L ratio and are able to conduct more current than nanowire FET's.

FIG. 7 illustrates a top view of a layout of nanofins for an array of nanofin transistors, according to various embodiments. The figure illustrates two "racetracks" of sidewall spacers 714, and further illustrates the portions of the sidewall spacers removed by an etch. The holes used to form the sidewall spacer

tracks were formed with a minimum feature size (1F). The mask strips 724 have a width of a minimum feature size (1F) and are separated by a minimum feature size (1F). In the illustrated layout, the columns of the nanofins have an approximately 2F center-to-center spacing, and the rows of the nanofins have an approximately 1F center-to-center spacing. Also, as illustrated in FIG. 7, since the nanofins are formed from sidewall spacers on the walls of the holes, the center-to-center spacing between first and second rows will be slightly less than 1F by an amount corresponding to the thickness of the nanofins (1F - ΔT), and the center-to-center spacing between second and third rows will be slightly more than 1F size by an amount corresponding to the thickness of the nanofins (1F + ΔT). In general, the center-to-center spacing between first and second rows will be slightly less than a feature size interval (NF) by an amount corresponding to the thickness of the nanofins (NF - ΔT), and the center-to-center spacing between second and third rows will be slightly more than a feature size interval (NF) by an amount corresponding to the thickness of the nanofins (NF + ΔT).

FIG. 8 illustrates a process to fabricate a nanofin transistor, according to various embodiments of the present subject matter. At 825, amorphous semiconductor fins are formed on a crystalline substrate and over a doped region that is to function as a first source/drain region. In some embodiments, the substrate is doped and diffused after the fins are formed. The fins are thin such that the dopant is able to diffuse under and into a bottom portion of the fin. The fins are crystallized at 826. A solid phase epitaxial (SPE) process is used, in which the structure is annealed and the crystalline substrate seeds crystalline growth in the fins. At 827, surrounding gate insulators are formed around the fins; and at 828, surrounding gates are formed around and separated from the fins by surrounding the gate insulators. The resulting structure is backfilled with an insulator at 829. Trenches are etched and gate line(s) are formed adjacent to and in contact with the surrounding gate, as illustrated at 830. At 831, a second source/drain region is formed in a top portion of the fins, and contacts for the second source/drain regions are formed at 832.

FIG. 9 illustrates a process to form amorphous semiconductor fins, such as illustrated at 825 in FIG. 8, according to various embodiments of the present subject matter. At 933, holes are etched in a first layer over a crystalline substrate. At 934, amorphous sidewall spacers are formed in each hole against the wall of the first layer for each hole. The first layer is removed at 935, which leaves the amorphous semiconductor fins on the crystalline substrate.

FIG. 10 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter. The illustrated memory device 1036 includes a memory array 1037 and read/write control circuitry 1038 to perform operations on the memory array via communication line(s) or channel(s) 1039. The illustrated memory device 1036 may be a memory card or a memory module such as a single inline memory module (SIMM) and dual inline memory module (DIMM). One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that semiconductor components in the memory array and / or the control circuitry can include nanofin transistors, as described above. The structure and fabrication methods for these devices have been described above.

The memory array 1037 includes a number of memory cells 1040. The memory cells in the array are arranged in rows and columns. In various embodiments, word lines 1041 connect the memory cells in the rows, and bit lines 1042 connect the memory cells in the columns. The read/write control circuitry 1038 includes word line select circuitry 1043 which functions to select a desired row, bit line select circuitry 1044 which functions to select a desired column, and read circuitry 1045 which functions to detect a memory state for a selected memory cell in the memory array 1037.

FIG. 11 illustrates a diagram for an electronic system 1146 having one or more nanofin transistors, according to various embodiments. Electronic system 1146 includes a controller 1147, a bus 1148, and an electronic device 1149, where the bus provides communication channels between the controller and the

electronic device. In various embodiments, the controller and/or electronic device include nanofin transistors as previously discussed herein. The illustrated electronic system 1146 may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

FIG. 12 depicts a diagram of an embodiment of a system 1250 having a controller 1251 and a memory 1252. The controller 1251 and/or memory 1252 may include nanofin transistors according to various embodiments. The illustrated system 1250 also includes an electronic apparatus 1253 and a bus 1254 to provide communication channel(s) between the controller and the electronic apparatus, and between the controller and the memory. The bus may include an address, a data bus, and a control bus, each independently configured; or may use common communication channels to provide address, data, and/or control, the use of which is regulated by the controller. In an embodiment, the electronic apparatus 1253 may be additional memory configured similar to memory 1252. An embodiment may include a peripheral device or devices 1255 coupled to the bus 1254. Peripheral devices may include displays, additional storage memory, or other control devices that may operate in conjunction with the controller and/or the memory. In an embodiment, the controller is a processor. Any of the controller 1251, the memory 1252, the electronic apparatus 1253, and the peripheral devices 1255 may include nanofin transistors according to various embodiments. The system 1250 may include, but is not limited to, information handling devices, telecommunication systems, and computers. Applications containing nanofin transistors, as described in this disclosure, include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

The memory may be realized as a memory device containing nanofin transistors according to various embodiments. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM). Various emerging memory technologies are capable of using nanofin transistors.

This disclosure includes several processes, circuit diagrams, and cell structures. The present subject matter is not limited to a particular process order or logical arrangement. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover adaptations or variations of the present subject matter. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing and understanding the above description. The scope of the present subject matter should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method for forming a transistor, comprising:

forming a transistor body, including:

forming a fin of amorphous semiconductor material on a crystalline substrate, the fin having a cross-sectional thickness in at least one direction less than a minimum feature size; and

performing a solid phase epitaxy (SPE) process to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth, the transistor body being formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region;

forming a surrounding gate insulator around the semiconductor pillar; and

forming a surrounding gate around and separated from the semiconductor pillar by the surrounding gate insulator.

2. The method of claim 1, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

3. The method of claim 1, wherein forming a fin of amorphous semiconductor material on a crystalline substrate includes forming a pillar of amorphous silicon on a crystalline silicon substrate.

4. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

5. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon gate.

6. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

7. The method of claim 1, further comprising forming the first source/drain region at a first end of the fin and forming the second source/drain region at a second end of the fin.

8. The method of claim 1, wherein the first source/drain region is beneath the second source/drain region, and a channel region is vertically oriented between the first and second source/drain regions.

9. A method for forming a transistor, comprising:

forming a silicon nitride layer on a silicon wafer;

etching a hole in the silicon nitride, the hole extending through the silicon nitride layer to the silicon wafer and being defined by the sides of the silicon nitride layer;

forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the hole;

removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer;

crystallizing the sidewall spacers;

masking and etching the sidewall spacers to form at least one silicon fin from the sidewall spacers, the silicon fin being positioned over a doped region to function as a first source/drain region for the transistor;

forming a surrounding gate insulator around the silicon fin;

forming a surrounding gate around and separated from the silicon fin by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the silicon fin.

10. The method of claim 9, wherein the height of the silicon fin is less than the minimum feature size.

11. The method of claim 9, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

12. The method of claim 9, wherein forming a surrounding gate insulator around the silicon fins includes performing a thermal oxidation process.

13. The method of claim 9, further comprising patterning and implanting the doped region to function as the first source/drain region before forming the amorphous silicon sidewall spacers.

14. The method of claim 9, wherein forming the surrounding gate includes forming a metal gate.

15. The method of claim 9, wherein forming the surrounding gate includes forming a polysilicon gate.

16. A method for forming an array of transistors, comprising:

forming buried source/drain regions in a silicon wafer;

etching a plurality of holes in a silicon nitride layer on the silicon wafer, the holes extending through the silicon nitride to the silicon wafer, each hole being defined by edges of the silicon nitride layer;

forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the holes;

removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer in a plurality of rectangular tracks;

crystallizing the sidewall spacers;

masking and etching the sidewall spacers to form a plurality of silicon fins from the sidewall spacers, the silicon fins being positioned over the buried source/drain regions;

forming a surrounding gate insulator around each of the silicon fins;

forming a surrounding gate around and separated from each of the silicon fins by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the silicon fins.

17. The method of claim 16, further comprising forming at least one gate line adjacent to and in contact with the surrounding gates for at least two transistors.

18. The method of claim 17, wherein forming at least one gate line includes forming two gate lines adjacent to and in contact with the surrounding gate, the two gate lines being on opposing silicon fins.

19. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a row of transistors.

20. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a column of transistors.

21. A transistor, comprising:

a crystalline substrate;

a crystalline semiconductor fin on the substrate, the semiconductor fin having a cross-sectional dimension that is less than a minimum feature size, wherein the fin provides a vertically-oriented channel between a lower source/drain region and an upper source/drain region;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

22. The transistor of claim 21, wherein the crystalline substrate is a silicon wafer.

23. The transistor of claim 21, wherein the gate insulator includes silicon oxide.

24. The transistor of claim 21, wherein the gate includes polysilicon.

25. The transistor of claim 21, wherein the gate includes metal.

26. A transistor, comprising:

a crystalline silicon substrate;

a first source/drain region formed in the crystalline silicon substrate;

a crystalline silicon fin on the substrate and over the first source/drain region, the silicon fin having a cross-sectional dimension that is less than a minimum feature size;

a second source/drain region formed in a top portion of the fin to define a vertically-oriented channel region in the fin between the first and second source/drain regions;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

27. The transistor of claim 26, wherein the gate insulator includes a silicon oxide.

28. The transistor of claim 26, wherein the silicon oxide gate insulator is a thermally-grown silicon oxide.

29. The transistor of claim 26, wherein the surrounding gate includes a polysilicon surrounding gate.

30. The transistor of claim 26, wherein the surrounding gate includes a metal surrounding gate.

31. A semiconductor structure, comprising:

an array of transistors arranged in columns and rows, each transistor including a first source/drain region, a second source/drain region above the first source/drain region, and a vertically-oriented channel region between the first and second source/drain regions, the channel region being formed in a crystalline semiconductor fin having a cross-sectional thickness that is less than a minimum feature size, each transistor further including a gate insulator formed around the fin and a surrounding gate formed around and separated from the fin by the gate insulator;

the columns of fin structures having a center-to-center spacing of approximately two minimum feature sizes; and

the rows of fins structures having a center-to-center spacing of approximately one minimum feature size.

32. The structure of claim 31, wherein a first row and an adjacent second row has a center-to-center spacing of the minimum feature size less the thickness of the fin structures, and the second row and an adjacent third row has a center-to-center spacing of the minimum feature size plus the thickness of the fin structures.

33. The structure of claim 31, wherein the fin structure has a long side and a short side, the structure further comprising at least one gate line adjacent to the long side.

34. The structure of claim 31, wherein the fin structure has a long side and a short side, the structure further comprising at least one gate line adjacent to the short side.

35. A semiconductor structure, comprising:

a crystalline substrate; and

a semiconductor fin structure formed on the substrate in contact with a first source/drain region, the semiconductor fin having a thickness cross-sectional dimension less than a minimum feature size, the semiconductor pillar having a crystallized bottom portion and an amorphous top portion indicative of a partially-completed solid phase epitaxy (SPE) process.

36. The structure of claim 35, wherein the substrate includes a silicon wafer, and the semiconductor fin structure including silicon.

37. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, the fins having a center-to-center spacing of approximately two minimum feature sizes between the columns of fin structures.

38. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, the fins having a center-to-center spacing of approximately one minimum feature size between the rows of fin structures.

39. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, a first row and an adjacent second row has a center-to-center spacing of a minimum feature size interval (NF) less the thickness of the fin structures, and the second row and an adjacent third row has a center-to-center spacing of the minimum feature size interval (NF) plus the thickness of the fin structures.