Description

This invention relates to a method for fabricating field-effect transistors and more particularly to a method for fabricating field-effect transistors having non-alloyed contacts.

Background of the Invention

Conventional field-effect transistors are fabricated using a three mask process. A first mask is used to define an area on a semiconductor wafer for each field-effect transistor by etching a material outside of the photoresist covering developed by using the mask and conventional photolithography techniques. The mesa which is developed through this etching defines the active area of each device and insulates a field-effect transistor from its adjacent neighbors. A second mask is then utilized to define the ohmic contacts which become the source and drain electrodes. After etching the metallic layer so as to define these contacts, the photoresist material deposited through use of the second mask must be removed since the photoresist material cannot withstand the high temperatures used to alloy the contacts. These temperatures are usually greater than 200 °C. After alloying the contacts a third mask is then used in order to define an area between the source and drain electrodes which will accommodate the gate structure of the field-effect transistor. Since this third mask must be optically aligned with the source and drain electrodes, it is typical to allow a 1 to 2μm separation between the gate structure and the source and drain electrodes. A higher speed field-effect transistor could be realized if an even closer tolerance could be obtained between the gate structure and the source and drain electrodes.

Summary of the Invention

A high-speed field-effect transistor having a self-aligned gate structure is obtained in accordance with the present invention as featured in claim 1 wherein only two masks are used in the fabrication of the field-effect transistor. A first is used as in the prior art to define mesas which consist of individual electrically isolated mounds on a semiconductor wafer. The wafer used in the present process must be one where contact is provided to the current channel through a non-alloyed contact. A second mask is used to lay down photoresist material both for the development of the source and drain contacts and for development of the gate structure. The present invention is based on the realization that the photoresist material need not be removed after the development of the source and drain contacts. Instead a metallic material is deposited over the entire wafer and this material deposits through the gap in the photoresist material created by the second mask in order to develop a Schottky gate contact to the semiconductor material. As a result a completely self-aligned gate electrode is provided with extremely close tolerance between the gate structure and the source and drain regions of the field-effect transistor.

Brief Description of the Drawing

The invention will be more readily understood after reading the following detailed description in combination with the drawings wherein:

FIGS. 1 through 7 are cross-sectional diagrams of a semiconductor wafer on which field-effect transistors are fabricated using the present invention, and

FIG. 8 is a top view of the electrode structure for each field-effect transistor.

Detailed Description

A cross-sectional diagram of a semiconductor wafer that can be used in the practice of the present invention is shown in FIG. 1. As shown in this figure, the epitaxially grown structure consists of a Gallium Arsenide (GaAs) substrate 10 followed by a GaAs buffer layer 11 which in turn is followed by an electron channel 12. In the wafer which was fabricated the electron channel 12 was a delta doped electron channel of the type described in U.S. patent application entitled "Field-Effect Transistor Having a Delta-Doped Ohmic Contact", Serial No. 871,249, filed June 6, 1986, by J.E. Cunningham, E.F. Schubert and W-T Tsang, which corresponds to EP-A-0 248 439. Channel 12 and the other layers shown in FIG. 1 were fabricated using a molecular beam epitaxial apparatus. The only essential element which the wafer must have in order to practice the present invention is a top non-alloyed contact layer 14. This top non-alloyed contact layer 14 can be achieved by any one of several prior art means. In the wafer fabricated, layer 14 was a delta doped non-alloyed ohmic contact of the type described in the article entitled "Delta doped Ohmic Contacts to N-GaAs", Applied Physics Letters, Vol. 49, 1986, E.F.Schubert et al., pp. 292-294. Layer 14 may also be provided by a narrow gap semiconductor material, for example, InAs on top of a GaAs, as described in the article entitled "Ohmic contacts to n-GaAs using graded band gap layers of $Ga_{1-x}In_xAs$ grown by molecular beam epitaxy", J. Vac. Sci. Technol., 19(3), Sept./Oct. 1981, J.M.Woodall et al., pp. 626-627.

Between the electron channel 12 and the non-alloyed contact layer 14 an additional doped layer 13 may be fabricated in order to reduce the effect of a parasitic resistance. This layer 13 may also consist of a homogeneous doped semiconductor or of a series of delta doped layers as in the present embodiment. It should be understood by those skilled in the art, however, that layer 13 is not absolutely necessary in order to fabricated a field-effect transistor.

After a semiconductor wafer of the type shown in FIG. 1 has been grown, a metallic layer 21 is deposited on the top surface by evaporation immediately after crystal growth to inhibit the formation of an undesired oxide layer between the non-alloyed contact layer 14 and metallic layer 21. The metal used in layer 21 should adhere quite well to the non-alloyed contact layer 14. In the present embodiment titanium is used for layer 21. An additional metallic layer 22 of a noble metal is deposited on top of metallic layer 21 in order to decrease the ohmic resistance provided by the metallic layers. In the wafer that was fabricated, gold was used for metallic layer 22. This noble metal also inhibits the formation of oxides on the top of the titanium layer 21.

A first mask is then utilized through conventional photolithography to establish a photoresist layer 23 over the metallic layer 22. This photoresist layer 23 is used to define areas on the semiconductor wafer which will correspond to the active regions of the field-effect transistors. Conventional etchants are then used to remove the material of metallic layers 21 and 22 and the semiconductor materials that are not covered by photoresist layer 23. In this way conventional mesa structures are developed which insulate one device on the wafer from adjacent devices. After the photoresist material of layer 23 has been dissolved the mesa structure that remains for each field-effect transistor is shown in FIG. 3. The use of the first mask in the present invention is identical to the use of a first mask in the conventional fabrication of field-effect transistors.

A second mask is then used through conventional photolithography techniques to establish a photoresist layer 41 over all of the wafer except for a gap over metallic layer 22, as shown in FIG. 4 This gap is the photoresist layer 41 is placed at a position which corresponds to the gap which will exist between the source and drain electrodes of the field-effect transistor. A conventional metallic etchant consisting of 13 grams of potassium iodide and 7 grams of iodine in 250 milliliters of water is then applied in order to etch metallic layers 22 and 21 that are present underneath the gap in photoresist layer 41. During this etching of the metallic layers a small undercut of about 0.05 to 0.2μm of the metallic layer occurs. In this way metallic layers 21 and 22 are separated into source electrode 51 and drain electrode 52 for each of the field-effect transistors as shown in FIG. 5. The GaAs material underneath the gap in photoresist layer 41 is then etched away in order to create a gap in the non-alloyed contact layer 14 and in the parasitic resistance layer 13 where such a layer is present. The gap created during this semiconductor etching process must be sufficient such that the only electrical connection between the source and drain electrodes is through the electron channel 12 and not through any upper layers used to provide an ohmic contact. A metallic layer 61 consisting of titanium is then deposited over the entire wafer to obtain a layer having a thickness of about 50 nm. This is followed by the deposit of a gold metallic layer 62 over the titanium layer 61 to obtain a layer of about 150 nm. During this deposition, the metallic materials of titanium and gold also deposit through the gap of photoresist layer 41 thereby forming a Schottky gate electrode 63 over the semiconductor material as shown in FIG. 6.

The photoresist material of layer 41 is then removed thereby removing all of the metallic layer 61 and 62 except that which has been deposited on the semiconductor material through the gap in photoresist layer 41. The resulting field-effect transistor is shown in FIG. 7. Since this gate electrode 63 has been deposited through the same gap in photoresist layer 41 that was used to create the source and drain electrodes, the lateral distance between the gate electrode and the source and drain regions is dependent only on the amount of undercutting which takes place during the above-described etchant steps. In the embodiment constructed this undercutting resulted in a lateral distance between the gate electrode and the source and drain regions of only 0.05 to 0.2μm. This small gate electrode tolerance is achieved in the present invention since a single mask has been utilized to develop the source and drain electrodes and the gate structure. The gate is self-aligned and this self-alignment has the advantages of keeping tolerances small and therefore keeping parasitic resistances small.

FIG. 8 shows a top view of the self-aligned field-effect transistor. As shown in FIG. 8 the gate electrode 63 is joined to a much larger pad 81 in order to facilitate connection to the gate electrode.

What has been described hereinabove is an illustrative embodiment of the present invention. For example, a combination of three metals consisting, for example, of titanium, platinum and gold could also be used in order to develop the gate electrode. Similarly other semiconductor materials could also be used in fabrication of the field-effect transistors.

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Claims

1. A method of fabricating Schottky gate field-effect transistors each having a source, drain and gate electrodes comprising the steps of epitaxially growing layers on a semiconductor substrate (10) including at least a current channel (12) followed by a non-alloyed contact layer (14) to form a semiconductor wafer, depositing a metallic layer (21;22) on said non-alloyed contact layer (14), masking regions (23) on the wafer corresponding to individual field-effect transistors using a first deposited photoresist layer and photolithography techniques, etching the metallic layer (21;22) and the epitaxially grown layers (12;14) to form mesas corresponding to individual field-effect transistors, dissolving said first deposited photoresist material, masking said wafer using photolithography and a second deposited photoresist layer (41) to define an area in each of the remaining portions of said metallic layer on the top of each mesa for the gate electrode structure of each field-effect transistor, etching the exposed area in each of the remaining portions of said metallic layer and the underlying non-alloyed contact layer, whereby the second deposited photorisist layer (41) is undercut, depositing a metallic contact layer (61;62) on the entire wafer including the defined areas to form a gate structure (63) in each defined area, and removing said second deposited photoresist layer (41) deposited thereby removing all of the metallic layer (61;62) except that which forms said gate structure (63).

2. A method as defined in claim 1 wherein the step of depositing a metallic layer on said non-alloyed contact layer (14) comprises the step of depositing a first metal layer on said non-alloyed contact layer in order to inhibit the formation of an undesired oxide layer, and depositing a second metal layer consisting of a noble metal on said first metal.

3. A method as defined in claim 1 wherein the step of depositing a metallic contact layer so as to form a gate structure comprises the steps of depositing a first metal contact layer that adheres well to semiconductor material, and depositing a second metal contact layer that consists of a metal having a low ohmic resistance.

Revendications

1. Procédé de fabrication de transistors à effet de champ à grille Schottky comportant chacun une électrode de source, une électrode de drain et une électrode de grille, comprenant les étapes qui consistent à former, par croissance épitaxiale, des couches sur un substrat semiconducteur (10), comprenant au moins un canal de courant (12) suivi par une couche de contact non allié (14), pour former une tranche de semiconducteur, à déposer une couche métallique (21; 22) sur la couche de contact non allié (14), à masquer des régions (23) sur la tranche correspondant à des transistors à effet de champ individuels, en utilisant une première couche de résine photosensible déposée, et des techniques de photogravure, à graver la couche métallique (21; 22) et les couches formées par croissance épitaxiale (12; 14), pour former des structures mésas correspondant à des transistors à effet de champ individuels, à dissoudre la première résine photosensible déposée, à masquer la tranche en utilisant une opération de photogravure et une seconde couche de résine photosensible déposée (41), pour définir une zone dans chacune des parties restantes de la couche métallique, sur la surface supérieure de chaque structure mésa, pour la structure d'électrode de grille de chaque transistor à effet de champ, à graver la zone à nu dans chacune des parties restantes de la couche métallique et dans la couche de contact non allié sous-jacente, ce qui a pour effet de provoquer une surgravure latérale par rapport à la seconde couche de résine photosensible déposée (41), à déposer une couche de contact métallique (61; 62) sur la totalité de la tranche, comprenant les zones définies, pour former une structure de grille (63) dans chaque zone définie, et à enlever la seconde couche de résine photosensible déposée (41), pour enlever ainsi la totalité de la couche métallique (61; 62) sauf celle qui forme la structure de grille (63).

2. Un procédé selon la revendication 1, dans lequel l'étape de dépôt d'une couche métallique sur la couche de contact non allié (14) comprend l'étape qui consiste à déposer une première couche de métal sur la couche de contact non allié, dans le but d'empêcher la formation d'une couche d'oxyde indésirable, et à déposer sur la première couche de métal une seconde couche de métal consistant en un métal noble.

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3. Un procédé selon la revendication 1, dans lequel l'étape de dépôt d'une couche métallique de façon à former une structure de grille comprend les étapes qui consistent à déposer une première couche de contact en métal qui adhère bien au matériau semiconducteur, et à déposer une seconde couche de contact en métal qui consiste en un métal ayant une faible résistance ohmique.

Patentansprüche

1. Verfahren zur Herstellung von Schottky-Gate-Feldeffekt-Transistoren, die je eine Source-, Drain- und Gate-Elektrode besitzen, mit den Verfahrensschritten:

Epitaktisches Aufwachsen von Schichten auf ein Halbleitersubstrat (10) einschließlich wenigstens eines Stromkanals (12) gefolgt durch eine nicht legierte Kontaktschicht (14) zur Bildung eines Halbleiterwafers,

Abscheiden einer metallischen Schicht (21,22) auf der nicht legierten Kontaktschicht (14),

Maskieren von Zonen (23) auf dem Wafer entsprechend den einzelnen Feldeffekt-Transistoren unter Verwendung einer ersten abgeschiedenen Fotoresistschicht und fotolitografischer Techniken,

Ätzen der metallischen Schicht (21,22) und der epitaktisch aufgewachsenen Schichten (12,14) zur Bildung von Mesas entsprechend den einzelnen Feldeffekt-Transistoren,

Auflösen der ersten niedergeschlagenen Fotoresistschicht,

Maskieren des Wafers unter Anwendung der Fotolitografie und Verwendung einer zweiten niedergeschlagenen Fotoresistschicht (41) zur Definierung eines Bereichs in jedem der restlichen Teile der metallischen Schicht auf der Oberseite jedes Mesa für die GateElektrodenstruktur jedes Feldeffekt-Transistors,

Ätzen des freigelegten Bereichs in jedem der restlichen Teile der metallischen Schicht und der darunter liegenden, nicht legierten Kontaktschicht, wodurch die zweite niedergeschlagene Fotoresistschicht (41) unterschnitten wird,

Abscheiden einer metallischen Kontaktschicht (61,62) auf dem gesamten Wafer einschließlich der definierten Bereiche zur Bildung einer Gate-Struktur (63) in jedem definierten Bereich und

Entfernen der zweiten niedergeschlagenen Fotoresistschicht (41), wodurch die gesamte metallische Schicht (61,62) mit Ausnahme der Teile, die die Gate-Struktur (63) bilden, entfernt wird.

2. Verfahren nach Anspruch 1, bei dem der Schritt des Abscheidens einer metallischen Schicht auf der nicht legierten Kontaktschicht (14) das Abscheiden einer ersten Metallschicht auf der nicht legierten Kontaktschicht zur Verhinderung der Bildung einer unerwünschten Oxydschicht und das Abscheiden einer zweiten, aus einem Edelmetall bestehenden Metallschicht auf dem ersten Metall vorsieht.

3. Verfahren nach Anspruch 1, bei dem der Schritt des Abscheidens einer metallischen Kontaktschicht zur Bildung einer GateStruktur das Abscheiden einer ersten metallischen Kontaktschicht, die gut auf dem Halbleitermaterial haftet, und das Abscheiden einer zweiten metallischen Kontaktschicht vorsieht, die aus einem Metall mit niedrigem Ohm'schen Widerstand besteht.