

COMPARATOR

This invention relates to comparators.

A conventional comparator generally has a
5 construction such as that shown in Figure 3 in which a
transistor T_3 is connected in series with a resistor R_3
and a transistor T_4 is connected in series with a
resistor R_4 . The junction of the transistor T_3 and the
resistor R_3 and the junction of the transistor T_4 and
10 the resistor R_4 are connected to inputs of a
differential amplifier A which produces an output
corresponding to the difference between the signals
supplied to the bases of the transistors T_3, T_4 .

In this arrangement, setting a comparison level is
15 performed by changing a reference potential in the case
of a single input while it is performed by changing
resistors R_3, R_4 in the case of a differential input.

The setting of the comparison level in the case of
the differential input will now be described. If the
20 difference between the inputs of the bases of the
transistors T_3, T_4 is represented by V_i , and a change in
current is represented by i , currents $(I + i)$, $(I - i)$
flow through the transistors T_3, T_4 , respectively, and
the respective collector potentials V_{t1c}, V_{t2c} are given
25 by:

$$V_{t1c} = V_{cc} - R_3 (I + i)$$

$$V_{t2c} = V_{cc} - R_4 (I - i)$$

Since $V_{t1c} = V_{t2c}$, the comparator starts to operate when the comparison level is:

$$i = I (R_4 - R_3) / (R_3 + R_4)$$

It can be seen from this equation that when, for example, $R_3 = R_4$, the comparator operates with $i = 0$, while when $R_4 = 2R_3$, the comparator operates with $i = I/3$. Namely, when $R_4 = 2R_3$, the comparator operates with application of an operating voltage v_1 thereto such that a current $i = I/3$ flows therethrough.

A drawback of this comparator is that when the comparison level is set with a reference voltage, the reference voltage and an input potential to be compared must be of high accuracy.

In the case of a differential input, as described above, the comparison level is determined by $(R_4 - R_3) / (R_3 + R_4)$, so that, disadvantageously, relative accuracy of the resistors is required, especially, when the resistances of the resistors R_3, R_4 are different.

According to the invention, there is provided a comparator comprising a first circuit including an integral number $\underline{m}$ of transistors (connected in parallel when $\underline{m} > 1$) to receive a first input signal to the respective bases of the transistor(s), a second circuit including an integral number $\underline{n}$ (where $\underline{n} \neq \underline{m}$) transistors (connected in parallel when $\underline{n} > 1$) to receive a second input signal to the respective bases of the transistor(s), a first load resistor connected in series with the first circuit, a second load resistor having the same resistance as the first resistor and connected in series with the second circuit, a series connected circuit including the first load resistor and the first circuit, a second series connected circuit including the second load resistor and the second circuit connectable in parallel with a power source, and a differential amplifier having input terminals connected to the junction of the first load resistor and the first circuit and the junction of the second load resistor and the second circuit.

According to a further aspect of the present invention, there is provided a comparator comprising a first circuit including an integral number $\underline{m}$ (where $\underline{m} > 1$) of transistors connected in parallel to receive a first input signal to the respective bases of the

transistors, a second circuit including an integral number $\underline{n}$ (where $\underline{n} < \underline{m}$) of transistors (connected in parallel when $\underline{n} > 1$) to receive a second input signal to the respective bases of the transistor(s), a third circuit including $(\underline{m} - \underline{n})$ transistors (connected in parallel when $(\underline{m} - \underline{n}) > 1$) to receive the second input signal to the bases of the transistors, a first load resistor through which, in operation, the first circuit is connected to a power source, a second load resistor having the same resistance as the first load resistor and through which, in operation, the second circuit is connected to the power source, the third circuit being connected in parallel with a series connected circuit including the second load resistor and the second circuit, and a differential amplifier having input terminals connected to the junction of the first load resistor and the first circuit and the junction of the second load resistor and the second circuit.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a circuit diagram of one embodiment of a comparator according to the present invention;

Figure 2 is a circuit diagram of another embodiment of a comparator according to the present invention; and

Figure 3 is a circuit diagram of a conventional comparator.

In Figure 1, there is shown one embodiment of a comparator according to the present invention in which
 5 $m(m = 1, 2 \dots)$ transistors T_1 are connected in parallel and an input terminal a is connected to the respective bases of the transistors. A load resistor R_1 is connected in series with the parallel arrangement of transistors. $n(n = 1, 2 \dots \text{ but } n \neq m)$ transistors T_2
 10 are connected in parallel and an input terminal b is connected to the respective bases of the transistors. A load resistor R_2 is also connected in series with the parallel arrangement of the transistors T_2 . The resistors R_1, R_2 , have the same resistance so as to
 15 facilitate integration. The junction of the resistor R_1 and transistors T_1 and the junction of the resistor R_2 and the transistors T_2 are connected to input terminals of a differential amplifier circuit A.

When a voltage V_i is applied across the input
 20 terminals a, b, assume that a change current i flows through each transistor and that a bias current $(m + n)I$ flows. A current $(I + i_1)$ flows through each transistor T_1 while a current $(I - i_2)$ flows through each transistor T_2 since:

$$m(I + i_1) + n(I - i_2) = (m + n)I$$

$$i_2 = (m/n)i_1.$$

If the collector voltages of the transistors T_1, T_2 are shown by V_{cm}, V_{cn} , respectively,

$$V_{cm} = V_{cc} - R m(I + i_1)$$

$$V_{cn} = V_{cc} - R n(I - m/n i_1).$$

Since $V_{cm} = V_{cn}$, the comparison level is given by

$$i_1 = ((n - m)/2m)I.$$

As just described, the comparison level is set by the numbers of the transistors T_1, T_2 . For example, when $n = 2$, and comparison is performed with $m = 1$, then $i_1 = I/2$, and $i_2 = I/4$.

The load resistors R_1, R_2 can be arranged to have the same value to set the comparison level. Therefore, the relative accuracy of the load resistors is easy to obtain and the structure is suitable for integration.

Another embodiment of a comparator according to the present invention will be described with reference to Figure 2. A first circuit includes $m(m = 1, 2 \dots)$ transistors T_1 connected in parallel with each other with an input terminal a being connected to the respective bases of the transistors. A first load resistor R_1 is connected in series with the parallel arrangement of the transistors T_1 . A second circuit includes $n(n = 1, 2 \dots$ where $n \neq m$) transistors T_2 with an input terminal b

being connected to the respective bases of the transistors. A second load resistor R_2 is connected in series with this parallel arrangement of the transistors T_2 . The resistors R_1, R_2 have the same resistance so as
 5 to render integration easy. The junction of resistor R_1 and transistor T_1 and the junction of resistor R_2 and transistor T_2 are connected to input terminals of a differential amplifier circuit A. In addition $(m - n)$ transistors T_3 , with the input terminal b connected to
 10 their respective bases, are connected in parallel with the resistor R_2 and the parallel arrangement of the transistors T_2 .

When a voltage V_1 is applied across the input terminals a, b, a current $(I - i_1)$ flows through each of
 15 the transistors T_1 and the current $(I + i_2)$ flows through each of the transistors T_2 and T_3 where i_1 and i_2 are change currents flowing through transistors T_1 and T_2 , respectively, and $2mI$ is the bias current. The following relationship holds from the point of view of
 20 the operational amplifier circuit A:

$$\begin{aligned} m(I - i_1) + n(I + i_2) + (m - n)(I + i_2) \\ = 2mI \end{aligned}$$

Therefore, $i_2 = i_1$.

If the collector voltages of the transistors T_1, T_2
 25 are V_{cm}, V_{cn} , respectively, then:

$$V_{cm} = V_{cc} - R_m(I - i_1)$$

$$V_{cn} = V_{cc} - R_n(I + i_1)$$

Since $V_{cm} = V_{cn}$, the comparison level is given by:

$$i_1 = \left(\frac{m}{m+n} - n \right) I / (m + n).$$

- 5 Thus, the comparison level is set in dependence upon the number of transistors T_1, T_2, T_3 . For example, when $m = 2$, $n = 1$, the comparison is performed with $i_1 = I/3$.

The comparison level can be set depending on the number of transistors used, so that the load resistors
 10 R_1, R_2 can have the same value, the relative accuracy of the resistors is easy to obtain and the structure is suitable for integration. Since the input DC biases can have the same voltage, the relative accuracy of biases is improved. In addition, quantities (absolute values)
 15 of changes in the collector currents to the input voltages, and bias currents in the respective transistors are the same, so that setting the respective comparison levels is relatively easy.

CLAIMS

1. A comparator comprising a first circuit including
an integral number $\underline{m}$ of transistors (connected in
5 parallel when $\underline{m} > 1$) to receive a first input signal to
the respective bases of the transistor(s), a second
circuit including an integral number $\underline{n}$ (where $\underline{n} \neq \underline{m}$)
transistors (connected in parallel when $\underline{n} > 1$) to
10 receive a second input signal to the respective bases of
the transistor(s), a first load resistor connected in
series with the first circuit, a second load resistor
15 having the same resistance as the first resistor and
connected in series with the second circuit, a series
connected circuit including the first load resistor and
the first circuit, a second series connected circuit
15 including the second load resistor and the second
circuit connectable in parallel with a power source,
and a differential amplifier having input terminals
connected to the junction of the first load resistor and
20 the first circuit and the junction of the second load
resistor and the second circuit.

2. A comparator comprising a first circuit including
an integral number $\underline{m}$ (where $\underline{m} > 1$) of transistors
connected in parallel to receive a first input signal to
25 the respective bases of the transistors, a second



circuit including an integral number $\underline{n}$ (where $\underline{n} < \underline{m}$) of transistors (connected in parallel when $\underline{n} > 1$) to receive a second input signal to the respective bases of the transistor(s), a third circuit including $(\underline{m} - \underline{n})$ transistors (connected in parallel when $(\underline{m} - \underline{n}) > 1$) to receive the second input signal to the bases of the transistors, a first load resistor through which, in operation, the first circuit is connected to a power source, a second load resistor having the same resistance as the first load resistor and through which, in operation, the second circuit is connected to the power source, the third circuit being connected in parallel with a series connected circuit including the second load resistor and the second circuit, and a differential amplifier having input terminals connected to the junction of the first load resistor and the first circuit and the junction of the second load resistor and the second circuit.

3. A comparator substantially as herein described with reference to Figure 1 of the accompanying drawings.

4. A comparator substantially as herein described with reference to Figure 2 of the accompanying drawings.



5. A comparator comprising: a first circuit including m ($m = 1, 2 \dots$) transistors connected in parallel and receiving a first input signal to the respective bases of the transistors; a second circuit including n ($n = 1, 2$
5 $\dots$ where $n \neq m$) connected in parallel and receiving a second input signal to the respective bases of the transistors; a first load resistor connected in series with the first circuit and a second load resistor having the same resistance with the first resistor and
10 connected in series with the second circuit; a series connected circuit including the first load resistor and the first circuit and a second series connected circuit including the second load resistor and the second circuit being connected in parallel with a power source;
15 and a differential amplifier having input terminals connected to the junction of the first load resistor and the first circuit and the junction the second load resistor and the second circuit.

6. A comparator comprising: a first circuit including
20 m ($m = 2, 3 \dots$) transistors connected in parallel and receiving a first input signal to the respective bases of the transistors; a second circuit including n ($n = 1, 2 \dots$ where $n < m$) transistors connected in parallel and receiving a second input signal to the respective bases
25 of the transistors; a third circuit including ($m - n$)



12

transistors connected in parallel and receiving the second input signal to the bases of the transistors; a first load resistor through which the first circuit is connected to a power source and a second load resistor

5 having the same resistance as the first load resistor and through which the second circuit is connected to the power source; a third circuit connected in parallel with a series connected circuit including the second load resistor and the second circuit; and a differential

10 amplifier having input terminals connected to the junction of the first load resistor and the first circuit and the junction of the second load resistor and the second circuit.

15

20

25