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(54) Title: A TRANSISTOR ARRANGEMENT AND A METHOD OF FORMING A TRANSISTOR ARRANGEMENT

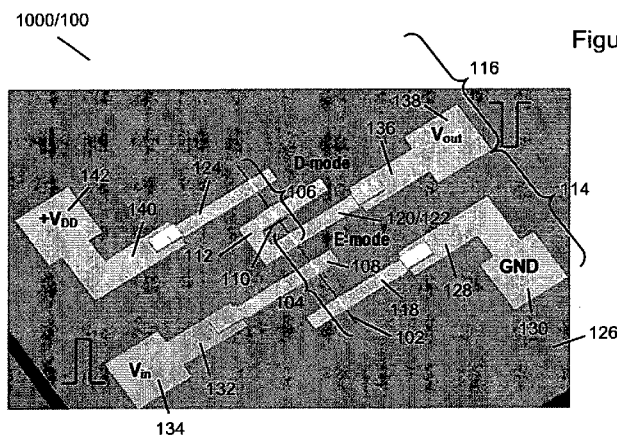


Figure 1A

(57) Abstract: In an embodiment, a transistor arrangement is provided. The transistor arrangement comprises a nanowire including a first nanowire region and a second nanowire region; a first gate contact disposed over the first nanowire region; an insulating region disposed over the second nanowire region; a second gate contact disposed over the insulating region; wherein the first nanowire region and the first gate contact forms a part of an enhancement mode transistor and the second nanowire region, the insulating region and the second gate contact forms a part of a depletion mode transistor. A method of forming a transistor arrangement may also be provided. Also contemplated is a transistor and a method for forming said transistor, where the transistor comprises a nanowire and a gate contact, where the gate contact is formed by directly writing the gate contact onto a region of the nanowire.