

Description

The invention relates to a sensor circuit for correlated double signal sampling, said sensor circuit comprising a sensor device having an output for supplying a sensor output signal, a sampling circuit coupled to the output of the sensor device for performing the sampling operation, and a clock pulse generator which is coupled to the sensor device and the sampling circuit for applying multi-phase control clock pulse signals thereto whereby an N-phase control clock pulse signal system is defined by a phase shift of 360° divided by N between the control clock pulse signals.

A sensor circuit of this type is known from an Article in the Journal "IEEE Journal of Solid-State Circuits" of February 1974, pp. 1 to 12. The sensor device suitable for pick-up is described as a charge-coupled device which is a specific implementation of a charge transfer device for generating a picture signal as the sensor output signal. To obtain an improved picture quality upon display, the correlated double signal sampling operation is performed during pixel periods. The double signal sampling implies that during a pixel period, firstly the signal is clamped on a reference voltage level via a series capacitor whereafter the actual signal sampling operation is performed with a storage of samples in a capacitor. In this way, as described, noise produced by a reset switch is removed, switching transients are eliminated and low-frequency noise is suppressed. A two phase control is described of a parallel-in, series-out sensor output register for supplying the sensor output signal and of the sampling circuit operating with two series of sampling pulses.

In current sensor devices the time difference between taking the two samples per pixel period is smaller or is of the order of 100 ns. This imposes strict requirements on the accuracy with which the sampling clock pulses are generated by the clock pulse generator.

Consequently, the components of the clock pulse generator must not have a large spread in signal delay times and should remain stable in time. A complicated and expensive clock pulse generator must be used in the sensor circuit.

The United States patent US-A-3,969,636 shows a charge sensing circuit for charge transfer devices in which a charge out of a "one phase" or "two phase" driven charge transfer device is collected by an inverting input of a differential amplifier and a capacitor connected between this inverting input and an output of the differential amplifier. The charge out of the charge transfer device will be cancelled by a same amount of charge delivered by the output of the differential amplifier via the capacitor, so that a voltage on the inverting input is kept constant and substantial equal to a voltage on the non inverting input. By sam-

pling a voltage on the output on an appropriate moment a measure for the amount of transferred charge becomes available. The charge on the capacitor is cancelled by closing a reset switch connected in parallel with the capacitor before a next sample of charge out of the charge transfer device can be accumulated. Operating this circuit involves a reset signal and a sample signal to be generated by a clock generator. Again a complicated and expensive clock generator must be used to guarantee the rigid coupling.

In the Japanese patent JP-A-61 50 364 a drive pulse of a final step of a CCD register and a reversed pulse of said drive pulse are used as a clamping and a sampling pulse of a correlated double sampling circuit for obtaining a rigid coupling between the clamping and sampling pulses and said drive pulse. The means to generate the derived pulse can introduce disturbances into the rigid coupling.

An object of the invention is *inter alia* to realise a sensor circuit comprising a simple and inexpensive clock pulse generator with which sufficiently accurate and stable clock pulses are generated for the sampling circuit. To this end, the invention provides a sensor circuit as defined in claim 1. Advantageous embodiments are defined in the dependent claims.

By directly deriving the sampling clock pulses via the clock pulse shaper from output transport clock pulses on two sensor clock pulse leads to control the supply of the sensor output signal, a rigid coupling is realised between this output signal and the sampling clock pulses. Variations, due to some cause or other, in the output transport clock pulses are immediately followed by the sampling clock pulses so that the two types of clock pulses are rigidly coupled with respect to the sensor output signal. Out of the clock generator no other signals than two of the already available control pulses are needed to generate, by simple means not sensitive to delay variations, these rigidly coupled sampling pulses.

The aspects of the invention will be described and elucidated in greater detail by way of non-limiting example with reference to the accompanying drawings in which

Fig. 1 is a circuit diagram of an embodiment of the sensor circuit according to the invention and Fig. 2 shows some time diagrams to illustrate the operation of the circuit of Fig. 1.

Fig. 1 shows a sensor device denoted by CTD having an output OT1 for the supply of a sensor output signal PS. A sampling circuit for correlated double sampling denoted by CDS is arranged between the sensor output OT1 and a sensor circuit output OT2. The sensor device CTD and the sampling circuit CDS are coupled to a clock pulse generator denoted by CG which is substantially implemented with a time signal generator TG and a clock pulse shaper CST according to the invention.

Fig. 1 shows by way of example a part of the sen-

sensor device CTD in the form of an integrated circuit. For details about the integrated circuit and the circuit diagram reference is made to Philips data relating to frame transfer sensors NXA 1111, 1121, 1131 and 1141. In fig. 1 a part of the sensor data has been taken over, namely a cross-section of an n, p, n-layer structure of a semiconductor body and some transistors T1, T2, T3 and T4 which are present in the integrated circuit. The said sensor device is shown by way of example but other forms are possible in a sensor circuit according to the invention.

In Fig. 1 the reference SR denotes a cross-section through a sensor output register of the integrated circuit. The register SR is shown with an n-substrate layer (n-sub), a p-layer and an n-layer. A more highly doped n^+ region is present in the n-semiconductor layer on which a sensor electrode ER is provided. The Figure also shows sensor electrodes E0, E1, E2 and E3 which are present on an electrically insulating layer IL provided on the semiconductor body. The transistors T1, T2, T3 and T4 are shown as MOS transistors which are of the n-type. The transistor T1 operating as a reset transistor is shown with a source electrode which is connected to the electrode ER, a drain electrode which receives a reset supply voltage V_{RD} and two gate electrodes one of which receives a reset gate signal RT from the generator TG. The electrode ER is also connected to the gate electrode of the transistor T2. The source electrode of the transistor T2 is connected to the drain electrode of the transistor T3 and to gate electrodes of the transistors T1 and T4. In this case the said reset operation is performed by means of a feedback (T2, T1). The drain electrodes of the transistors T2 and T4 are connected to a supply voltage V_{DD} . The gate electrode of the transistor T3 is connected to its source electrode and both are connected to ground. The source electrode of the transistor T4 is connected to the sensor output OT1. Fig. 1 shows that the electrode E0 receives a supply voltage V_{OG} and E0 is operative as an output gate electrode at the integrated circuit. The supply and control voltages are considered to come from sources whose terminals (not shown) are connected to ground.

The electrodes E1, E2 and E3 of Fig. 1 are connected to sensor clock pulse leads C1, C2 and C3, respectively, which convey similarly denoted multi-phase control clock pulse signals, namely three-phase signals supplied by the generator TG. The leads C1, C2 and C3 extend across and in the part (not shown) of the register SR and are connected in this register to sensor electrodes E1, E2 and E3, respectively. It is assumed for the electrode sets (E1, E2, E3) that they are associated with sensor elements to be indicated similarly. The sensor element shown (E2, E3, E1) is the last in a row of transporting sensor elements in the shift register SR, an induced transistor being present under their electrodes E. In this case

any sensor element can be described with an input portion under electrode E2, a central portion under electrode E3 and an output portion under electrode E1. At the transport in the shift register SR a row of successively induced transistors thus occurs under electrode sets (E2, E3, E1), (E3, E1, E2), (E1, E2, E3), (E2, E3, E1) and so forth. For the three-phase control there are the three sensor element portions and for a four-phase control there are four sensor element portions under series of four electrodes E. For the sake of completeness of the description it is to be noted that the last induced transistor in the shift register SR occurs under the electrode set (E1, E0, ER), the electrode E1 being operative as a switching electrode. After a reset by the transistor T1 an information charge occurs under the electrode ER via the switching electrode E1, which charge ultimately leads to the pixel information in the sensor output signal PS.

The known sampling circuit CDS following the sensor output OT1 is shown diagrammatically with a series capacitor C1', a subsequent switch S1 with a connection to ground, a series switch S2 and a capacitor C2' arranged between the sensor circuit output OT2 and ground. The control of the switches S1 and S2 is diagrammatically denoted by means of a broken line. The switches S1 and S2 are assumed to be electronic switches.

According to one aspect of the invention the control clock pulse signals for the sampling circuit CDS are not received from the time signal generator TG but are supplied by the clock pulse shaper CST. Two inputs CT1 and CT2 of the clock pulse shaper CST are coupled to the clock pulse leads C1 and C3, respectively, conveying the similarly denoted output transport clock pulses, and two outputs ST1 and ST2 are coupled to the switches S1 and S2, respectively, of the sampling circuit CDS.

In the clock pulse shaper CST the inputs CT2 and CT1 are coupled to control electrodes of semiconductor switching elements T5 and T6, respectively, shown in Fig. 1 as (n)MOS transistors with gate electrodes g as control electrodes. The transistors T5 and T6 are connected to ground by means of inputs indicated as source electrodes s. Drain electrodes d operating as outputs of the transistors T5 and T6 are coupled to the outputs ST1 and ST2, respectively, of the clock pulse shaper CST. The control electrode g of the transistor T6 and the input CT1 connected to it have a DC coupling to the other output ST1 via a parallel arrangement of a resistor R1 and a diode D. The output ST1 is assumed to have a parasitic capacitance Cp1 to ground. The control electrode g of the transistor T5 and the input CT2 connected to it have a DC coupling with the other output ST2 via a resistor R2. The output ST2 is assumed to have a parasitic capacitance Cp2 to ground. While supplying the output transport clock pulses C1 and C3 to the respective inputs CT1 and CT2, the clock pulse shaper CST sup-

plies sampling clock pulses CL and SA to the respective outputs ST1 and ST2.

To illustrate the operation of the sensor circuit of Fig. 1, Fig. 2 shows some time diagrams for the output transport clock pulse signals C1, C2 and C3, the sensor output signal PS and the sampling clock pulse signals CL and SA. The clock pulses are plotted as a function of time t with a variation between the ground potential of OV and a voltage level Va. A reference voltage level denoted by Vref is shown at the known signal PS. A signal value associated with a sensor pixel is denoted by V_{PS} . Dependent on a black, grey or white value of the pixel, the voltage difference between Vref and V_{PS} is small, larger or largest. The references t_0 , t_1 , t_2 , t_3 and t_4 denote some instants. The instants t_0 and t_4 are shown as a starting instant and a final instant, respectively, of a pixel period TP to be described. The signals of Fig. 2 will be described without allowing for voltage drops across the transistors T5 and T6 and the diode D of Fig. 1.

Between instants t_0 and t_1 , it holds that $C1 = Va$ and $C3 = Va$, in which case the transistors T6 and T5 of Fig. 1 are turned on, so that the ground potential of OV occurs in the signals CL and SA of Fig. 2.

At the instant t_1 , $C3 = Va$ changes into $C3 = OV$. As a result, the transistor T5 is turned off and due to $C1 = Va$ a charge current will flow through the resistor R1 to the capacitance Cp1. Due to the charge supply to the capacitance Cp1 with a time constant which is equal to $R1 \cdot Cp1$, the leading edge of the signal CL of Fig. 2 has the variation shown. The transistor T6 which remains turned on due to $C1 = Va$ causes SA to remain OV. The operation is illustrated by means of crosses at C1 and C3.

At the instant t_2 , $C1 = Va$ changes into $C1 = OV$. As a result, the capacitance Cp1 is immediately discharged across the diode D which implies a quick depletion of charge. An arrow head at the signal C1 illustrates the operation.

Between the instants t_2 and t_3 , it holds that $C1 = OV$ and $C3 = OV$ in which case the ground potential of OV occurs at the outputs ST1 and ST2 conveying the respective signals CL and SA via the respective resistors R1 and R2.

At the instant t_3 , $C3 = OV$ changes into $C3 = Va$. Since the transistor T6 is turned off at $C1 = OV$, $C3 = Va$ supplies a charge current through the resistor R2 to the capacitance Cp2 so that there is a charge supply with a time constant which is equal to $R2 \cdot Cp2$. The signal SA of Fig. 2 shows the variation. In this case $C1 = OV$ remains valid, while $CL = OV$ and the transistor T6 remains turned off.

At the instant t_4 , $C1 = OV$ changes into $C1 = Va$. As a result, the transistor T6 is immediately turned on and the capacitance Cp2 is discharged with a quick depletion of charge. The next pixel period starts at the instant t_4 .

Fig. 2 shows the sampling clock pulses in the sig-

nal CL for the signal clamping and in the signal SA for the actual signal sampling, which have an effective instant just before the instants t_2 and t_4 , respectively. This means that the state in the signal PS just before the instant t_2 is decisive of the signal clamping at the reference voltage level Vref and that the state just before the instant t_4 is decisive of the sampling value. These instants t_2 and t_4 are accurately fixed at the signals CL and SA by the signal C1 (illustrated by means of the arrow heads), the signal C3 occurring as a preparatory signal, as is comparable with flip-flop circuits having trigger and preparatory inputs. A rigid coupling is realised between the signals shown in Fig. 2, with the instants t_2 and t_4 being decisive.

The clock pulse shaper CST of Fig. 1 is shown in an embodiment using the output transport clock pulse signals C1 and C3. This embodiment can be further applied if the inverted signal C2 instead of the signal C3 is utilized for shaping the sampling clock pulses according to Fig. 2. In this case sampling clock pulses in the signals CL and SA are generated with half a period, namely a period of $1/6$ TP. The slope of the leading edges of the sampling clock pulses must be such that the sampling is not influenced by, for example, too slow switches S1 and S2 of Fig. 1. The choice of the clock pulse signals C1 and C3 is the safest for generating the clock pulses in the signals CL and SA with a period of $1/3$ TP.

In the case of a four-phase clock pulse control (C1, C2, C3, C4) of the shift register SR, the instants t_2 and t_4 shown in Fig. 2 determine the trailing edges of the pulses in the signals CL and SA in an unmodified form. When applying the transport clock pulse signals C1 and C4 to the clock pulse shaper CST of Fig. 1, instants t_1' and t_3' occur at $1/4$ and $3/4$ of the pixel period TP. The clock pulses in the signals CL and SA have a period of $1/4$ TP.

It is apparent from the foregoing that at least a three-phase control system must be present for the choice of two output transport clock pulse signals.

Claims

1. A sensor circuit for correlated double signal sampling, said sensor circuit comprising a sensor device (CTD) having an output (OT1) for supplying a sensor output signal (PS), a sampling circuit (CDS) coupled to the output (OT1) of the sensor device (CTD) for performing a sampling operation, and a clock pulse generator (TG) which is coupled to the sensor device (CTD) and the sampling circuit (CDS) for applying multi-phase control clock pulse signals (C1, C2, C3) thereto whereby an N-phase control clock pulse signal system is defined by a phase shift of 360° divided by N between the control clock pulse signals, characterized in that

plies sampling clock pulses CL and SA to the respective outputs ST1 and ST2.

To illustrate the operation of the sensor circuit of Fig. 1, Fig. 2 shows some time diagrams for the output transport clock pulse signals C1, C2 and C3, the sensor output signal PS and the sampling clock pulse signals CL and SA. The clock pulses are plotted as a function of time t with a variation between the ground potential of OV and a voltage level Va. A reference voltage level denoted by Vref is shown at the known signal PS. A signal value associated with a sensor pixel is denoted by V_{PS} . Dependent on a black, grey or white value of the pixel, the voltage difference between Vref and V_{PS} is small, larger or largest. The references t_0 , t_1 , t_2 , t_3 and t_4 denote some instants. The instants t_0 and t_4 are shown as a starting instant and a final instant, respectively, of a pixel period TP to be described. The signals of Fig. 2 will be described without allowing for voltage drops across the transistors T5 and T6 and the diode D of Fig. 1.

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At the instant t_2 , $C1 = Va$ changes into $C1 = OV$. As a result, the capacitance Cp1 is immediately discharged across the diode D which implies a quick depletion of charge. An arrow head at the signal C1 illustrates the operation.

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The clock pulse shaper CST of Fig. 1 is shown in an embodiment using the output transport clock pulse signals C1 and C3. This embodiment can be further applied if the inverted signal C2 instead of the signal C3 is utilized for shaping the sampling clock pulses according to Fig. 2. In this case sampling clock pulses in the signals CL and SA are generated with half a period, namely a period of $1/6$ TP. The slope of the leading edges of the sampling clock pulses must be such that the sampling is not influenced by, for example, too slow switches S1 and S2 of Fig. 1. The choice of the clock pulse signals C1 and C3 is the safest for generating the clock pulses in the signals CL and SA with a period of $1/3$ TP.

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It is apparent from the foregoing that at least a three-phase control system must be present for the choice of two output transport clock pulse signals.

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the clock pulse generator (TG) comprises at least three sensor clock pulse leads (C1,C2,C3) for supplying an at least three-phase control pulse (C1,C2,C3) to control the sensor output signal (PS), and a clock pulse shaper (CST) having two inputs (CT1,CT2) and two outputs (ST1,ST2), the two inputs (CT1,CT2) being coupled to two of the at least three sensor clock pulse leads (C1,C2,C3) said two sensor clock pulse leads carrying control clock pulses being mutually phase-shifted but not in antiphase and the two outputs (ST1,ST2) being coupled to the sampling circuit (CDS).

2. A sensor circuit as claimed in claim 1, characterized in that the clock pulse shaper (CST) comprises two transistors (T5,T6), and each input (CT1,CT2) of the clock pulse shaper (CST) is coupled to a respective control electrode (g) of the transistors (T5,T6) each having an output (d) coupled to one of the two clock pulse shaper outputs (ST1,ST2), each control electrode (g) having a DC coupling (R1,D;R2) with the other clock pulse shaper output (ST1,ST2).
3. A sensor circuit as claimed in claim 2, characterized in that one (R1,C) of said DC couplings (R1,C;R2) comprises a parallel arrangement of a resistor (R1) and a diode (D) for supplying charge to and depleting charge from the respective clock pulse shaper output (ST1).

Patentansprüche

1. Sensorschaltung für korrelierte doppelte Signalabtastung, wobei diese Schaltungsanordnung eine Sensoranordnung (CTD) aufweist mit einem Ausgang (OT1) zum Liefern eines Sensorausgangssignals (PS), mit einer mit dem Ausgang (OT1) der Sensoranordnung (CTD) gekoppelten Abtastschaltung (CDS) zum Durchführen eines Abtastvorgangs, und mit einem Taktimpulsgenerator (TG), der mit der Sensoranordnung (CTD) sowie mit der Abtastschaltung (CDS) gekoppelt ist zum derselben Liefern von Mehrphasenstuartaktimpulssignalen (C1,C2,C3), wobei ein N-Phasenstuartaktimpulssystem durch eine Phasenverschiebung von 360° geteilt durch N zwischen den Stuartaktimpulssignalen definiert wird, dadurch gekennzeichnet, daß der Taktimpulsgenerator (TG) wenigstens drei Sensortaktimpulsleitungen (C1, C2, C3) aufweist zum Liefern eines wenigstens Dreiphasensteuerimpulses (C1,C2,C3) zur Steuerung des Sensorausgangssignals (PS), und einen Taktimpulsformer (CST) mit zwei Eingängen (CT1, CT2) und zwei Ausgängen (ST1, ST2), wobei die beiden Eingän-

ge (CT1, CT2) mit zwei der wenigstens drei Sensortaktimpulsleitungen (C1,C2,C3) gekoppelt sind, wobei die genannten zwei Sensortaktimpulsleitungen mit den Stuartaktimpulsen gegenseitig phasenverschoben aber nicht gegenphasig sind, und wobei die beiden Ausgänge (ST1, ST2) mit der Abtastschaltung (CDS) gekoppelt sind.

2. Sensorschaltung nach Anspruch 1, dadurch gekennzeichnet, daß der Taktimpulsformer (CST) zwei Transistoren (T5,T6) aufweist, und jeder Eingang (CT1,CT2) des Taktimpulsformers (CST) mit einer betreffenden Steuerelektrode (g) der Transistoren (T5,T6) gekoppelt ist, von denen je ein Ausgang (d) mit einem der beiden Taktimpulsformerausgänge (ST1,ST2) gekoppelt ist, wobei jede Steuerelektrode (g) eine Gleichstromkopplung (R1,D;R2) mit dem anderen Taktimpulsformerausgang (ST1,ST2) hat.
3. Sensorschaltung nach Anspruch 2, dadurch gekennzeichnet, daß eine (R1,C) der genannten Gleichstromkopplungen (R1,C;R2) eine Parallelschaltung eines Widerstandes (R1) und einer Diode (D) aufweist zum Liefern von Ladung zu dem betreffenden Taktimpulsformerausgang (ST1) bzw. zum Entnehmen von Ladung daran.

Revendications

1. Circuit capteur pour échantillonnage de signal double à corrélation, ledit circuit capteur comprenant un capteur (CTD) ayant une sortie (OT1) pour fournir un signal de sortie de capteur (PS), un circuit d'échantillonnage (CDS) couplé à la sortie (OT1) du capteur (CTD) pour exécuter une opération d'échantillonnage, et un générateur d'impulsions d'horloge (TG) qui est couplé au capteur (CTD) et au circuit d'échantillonnage (CDS) pour y appliquer des signaux d'impulsions d'horloge de commande multiphase (C1, C2, C3), un système de signaux d'impulsions d'horloge de commande à N phases étant défini par un décalage de phase de 360° divisé par N entre les signaux d'impulsions d'horloge de commande, caractérisé en ce que le générateur d'impulsions d'horloge (TG) comprend au moins trois conducteurs d'impulsions d'horloge de capteur (C1, C2, C3) pour fournir une impulsion de commande au moins triphasée (C1, C2, C3) afin de commander le signal de sortie de capteur (PS), et un conformateur d'impulsions d'horloge (CST) ayant deux entrées (CT1, CT2) et deux sorties (ST1, ST2), les deux entrées (CT1, CT2) étant couplées à deux des au moins trois conducteurs d'impulsions d'horloge de capteur (C1, C2, C3), lesdits



deux conducteurs d'impulsions d'horloge de capteur acheminant des impulsions d'horloge de commande étant mutuellement déphasés, mais n'étant pas en opposition de phase, et les deux sorties (ST1, ST2) étant couplées au circuit d'échantillonnage (CDS). 5

2. Circuit capteur selon la revendication 1, caractérisé en ce que le conformateur d'impulsions d'horloge (CST) comprend deux transistors (T5, T6) et chaque entrée (CT1, CT2) du conformateur d'impulsions d'horloge (CST) est couplée à une électrode de commande respective (g) des transistors (T5, T6) ayant chacun une sortie (d) couplée à l'une des deux sorties (ST1, ST2) du conformateur d'impulsions d'horloge, chaque électrode de commande (g) ayant un couplage en courant continu (R1, D; R2) avec l'autre sortie (ST1, ST2) du conformateur d'impulsions d'horloge. 10 15 20

3. Circuit capteur selon la revendication 2, caractérisé en ce que l'un (R1, C) desdits couplages en courant continu (R1, C; R2) comprend un montage en parallèle d'une résistance (R1) et d'une diode (D) pour fournir de la charge et appauvrir en charge la sortie respective (ST1) du conformateur d'impulsions d'horloge. 25 30

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