

SEMICONDUCTOR DEVICE WITH BIASED FEATURE**ABSTRACT**

A transistor including a gate structure with a first portion and a second portion; the first and second portions each have a first edge and an opposing second edge that are substantially collinear. The gate structure also includes an offset portion interposing the first portion and the second portion. The offset portion has a third edge and an opposing fourth edge. The third edge and the fourth edge are non-collinear with the first and second edges of the first and second portions of the gate structure. For example, the offset portion is offset or shifted from the first and second portions.

FIG. 5