A RECEIVER FOR A PAGING SYSTEM

This invention relates to a receiver for a paging system for informing the user, for example by means of an audible sound or a display, that he or she has been called by radio from a transmitting station.

A radio paging system for broadcasting a call (paging) by means of a radio using a sub-carrier or an ordinary FM broadcasting wave is known for example from Japanese Laid Open Patent Publication No. 63-158924. In this type of paging system, a message is transmitted using a frequency within a frequency band that is assigned to a plurality of FM broadcasting stations, namely 87.6 MHz to 108.0 MHz, and each receiver has a scanning mode for automatically scanning the frequency band in order to determine the broadcast frequency of such message.

Since a radio paging receiver is at all times carried by the user and is taken to various places under a variety of conditions, it needs to have the capability of receiving a message reliably at any time and under any condition. Accordingly, in the final stage of production, tests for measuring the receiving characteristic of a receiving circuit within the receiver have to be carried out, followed by adjustment of the components thereof based on the results of such tests. Each test has to be carried out in accordance with a normal receiving operation by instigating a scanning mode, in which scanning within a pre-determined frequency band is carried out, to determine a specific frequency and by then transmitting paging data (a message) by radio transmission at the specific frequency determined in the scanning mode. As a result, the

scanning mode has to be repeated for every new test commenced by variously changing the environmental conditions, causing the problem that considerable time and labour is required for the testing and the accompanying adjustments.

This invention seeks to avoid or reduce the above problem and has for its object the provision of a receiver for a paging system in which testing during production involves substantially reduced time and labour.

According to the present invention, there is provided a receiver for a paging system, in which a specific frequency for receiving paging data supplied by radio transmission is determined by scanning through a pre-determined frequency band, said receiver comprising a receiving circuit in which a receiving frequency is selectively settable, operation means for generating an instruction to start a receiving characteristic test, and control means responsive to the start instruction to initiate a testing mode by initialising the receiving frequency of said receiving circuit to a previously defined test starting frequency without scanning.

Since the receiving frequency of the receiving circuit is instantly initialised to a previously defined test starting frequency when a start instruction is issued, the time previously required for a scanning operation is eliminated and the time needed for a receiving characteristic test is thus reduced. As a result, receiving characteristic tests and the

accompanying adjustments may be carried out efficiently and at reduced cost.

The invention is described further, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a block diagram of a receiver for a paging system according to the present invention;

Figure 2 is a flow chart representing the operation of the receiver in a testing mode;

Figure 3 is a flow chart representing the operation of the receiver in a normal receiving mode;

Figure 4 is a timing chart for explaining the operation of the receiver when a shift is made to a main testing stage of the testing mode;

Figure 5 is a timing chart for explaining the operation of the receiver when a shift is made to a preparatory stage of the testing mode;

Figure 6 is a front view of a display element showing a display during the testing mode; and

Figure 7 is a front view of the display element showing a display during a power off mode.

Figure 1 is a block diagram of a receiver for a paging system according to this invention, comprising an antenna 1, and an FM receiving circuit 2 for FM broadcast waves received by the antenna 1. The FM receiving circuit 2 comprises a known digital synthesiser tuner, which employs a PLL (phase locked loop) circuit and whose receiving frequency may be set voluntarily at every 0.1 MHz within the range 87.6 MHz to 108.0 MHz on the basis of receiving frequency data FD. The FM receiving circuit 2 may be changed between three different modes: a power off mode in which the supply of power is completely shut off; a power on mode in which power is supplied and reception is possible;

and a power saving mode in which reception is not possible and only certain minimum necessary functions, such as the setting of a receiving frequency, can be effected so as to reduce the power consumption. A change over between these modes is achieved by means of a power supply control signal C1 supplied from a power supply control circuit 9 which will be described later.

An FM base band signal output by the FM receiving circuit 2 is supplied to a decoder 3, and paging data (digital data) multiplexed in the FM sub-carrier frequency band is extracted by the decoder 3. After being subjected to error correction processing, the paging data is supplied as demodulation data DD to a controller 4.

The controller 4 is constructed as a single chip micro-computer and mainly comprises: a CPU (central processing unit) 5 for controlling the operation of each circuit portion; a ROM (read only memory) 6 in which programs to be executed by the CPU 5 and identification data for identifying a first test packet (TP1) and a second test packet (TP2), which will be described later, are stored; a RAM (random access memory) 7 in which various data is temporarily stored during the execution of a programme; and an I/O circuit 8 connected to the CPU 5 via a bus line for controlling the transfer of various items of data. In addition, the controller 4 further includes: the power supply control circuit 9 for supplying power supply control signals C1 and C2 to the FM receiving circuit 2 and the decoder 3, respectively, in accordance with instructions from the CPU 5; an oscillator circuit 10 for generating clock pulses ø as a reference for the operation of the CPU 5; and an LCD (liquid crystal display) driver 11 for driving an LCD 12 in accordance with display operation

instructions from the CPU 5.

In addition, the receiver includes a buzzer driver 13 which drives a buzzer 14 in accordance with a buzzer driving signal BS supplied from the controller 4, to generate a warning sound to draw the user's attention. A switch circuit 15 supplies to the controller 4 switch data SD according to an operation of push button type switches, namely A-switch 16A, B-switch 16B, C-switch 16C and D-switch 16D. A PROM programmable ROM) 17 stores a private call number assigned to each receiver of the paging system.

Operation of the receiver will now be described.

1. Testing mode.

A testing mode is initiated when testing is carried out as part of a factory shipping inspection for the receiver.

As a preparatory stage in such testing, a first test packet T1 is tranmitted from a testing transmitter by means of an FM transmitting wave at a pre-determined frequency of 88.1 MHz (designated a test starting frequency). This first test packet includes frequency data relating to the frequency (designated a first testing frequency) by which a next transmission will be made. Thereafter, as a main testing stage, a second test packet TP2 is transmitted repeatedly at fixed intervals by an FM transmitting wave at the first testing frequency. During the main testing stage, the receiving characteristic of the receiver at the first testing frequency is verified in dependence upon the number of time that the paging receiver has been able to receive the second test packet TP2. Next, for changing the testing frequency, the receiver is returned to the preparatory stage, in which a first test packet TP1 is

transmitted including frequency data relating to the frequency (designated a second testing frequency) by which the next transmission will be made, and then proceeds again to the main testing stage.

In this way, by repeating a preparatory stage and a main testing stage alternately, the receiving characteristics at respective testing frequencies, namely the first testing frequency, the second testing frequency, ..., are sequentially measured.

The operation of the paging receiver based on such testing will now be described with reference to Figure 2.

First, when the A-switch 16A, the B-switch 16B and the C-switch 16C are concurrently pressed, corresponding switch data SD is supplied to the CPU 5. Upon receipt of the switch data SD, the CPU 5 is switched from a normal receiving mode to a testing mode. Then, at step SP1 as shown in Figure 2, all the segments of LCD 12 are lit as shown in Figure 6 to indicate the testing mode. At the next step SP2, frequency data FD is supplied to the FM receiving circuit 2 to initialise the receiving frequency to 88.1 MHz, which is the test starting frequency. In this case, the FM receiving circuit 2 is in the power saving mode.

Next, at step SP3, the CPU 5 gives an instruction to the power supply control circuit 9 so as to switch the FM receiving circuit 2 from the power saving mode to the power on mode for a time period of about 30 msec to 40 msec in every second. The FM receiving circuit 2 thereby intermittently effects the receiving operation with a cycle constituted by a time period T1 (one second), as shown in Figure 4 (a).

In each performance of the receiving operation at step SP3, the program proceeds to the next step SP4 at

which the CPU 5 detects, on the basis of demodulation data DD, whether a first test packet TP1 has been received. If, in this step SP4, it is judged that a first test packet TP1 has not been received, the program proceeds to step SP5, in which a check is made as to whether a two minutes interval has passed. If the two minutes has not yet passed, the operation for detecting a first test packet TP1 is repeated by returning to step SP3. If a first test packet TP1 has still not been received after the two minutes, the program proceeds to step SP6, in which the FM receiving circuit 2 is switched to the power off mode. As shown in Figure 7, the characters "OFF" are displayed by the LCD 12 so as to indicate the power off mode.

In this way, the receiver is pre-adapted to ensure that an internal battery, the power source for the paging receiver is not wastefully used due to prolongation of the power on mode, for example following completion of the testing mode as a result of a first test packet TP1 not being received.

On the other hand, if the first test packet TP1 is received in step SP4, the program proceeds to step SP7. Then, the CPU 5 supplies the buzzer driving signal BS to the buzzer driver 13 for the time period T1 (one second) as shown in Figure 4 (c) to cause a warning sound (a prolonged tone) to be generated, indicating that a first test packet has been received. Next, the program proceeds to step SP8 in which the CPU 5 switches the FM receiving circuit 2 to the power off mode for a time period T3 (four seconds) as shown in Figure 4 (a) so as to suspend the receiving operation. The program then proceeds further to step SP9 in which the receiving frequency of the FM receiving circuit 2 is up-dated to the frequency (first testing frequency) by which the

next transmission will be made, on the basis of the frequency data included in the first test packet. In this way, the preparatory stage is completed.

During the four seconds of the time period T3, the transmitting frequency is changed at the location of the testing transmitter to the first testing frequency, and a shift is effected to a main testing stage in which a second test packet is repeatedly transmitted at fixed intervals by an FM transmitting wave at the first testing frequency.

Next, at step SP10, the CPU 5 re-sets to zero the count values in count areaa A1 and A2 of the RAM 7, which areas A1 and A2 are provided respectively for storing a number N of receiving operations effected and the number M of second test packets received. At the next step SP11, the CPU 5 causes the characters "TEST" to be displayed by the LCD 12 and also causes the count values corresponding to the number N of receiving operations effected and the number M of second test packets received to be displayed. Then, at step SP12, the CPU 5 gives an instruction to the power supply control circuit 9 to switch the FM receiving circuit 2 from the power saving mode to the power on mode for a time period of about 30 msec to 40 msec in every 0.5 seconds, whereby a receiving operation is intermittently carried out by the FM receiving circuit 2 with a cycle constituted by a time period T2 (0.5 sec) as shown in Figure 4 (a). On each execution of the receiving operation in step SP12, the program proceeds to the next step SP13 and increments by "1" the count value N corresponding to the number of receiving operations effected. Thereafter, the program proceeds to step SP14 in which the CPU5 provides the buzzer driving signal BS to the buzzer driver 13 for a time period T4

(< T2/2) as shown in Figure 4 (c) to cause a warning sound (a short tone) to be generated, indicating that a receiving operation has been performed. Next, at step SP15, the CPU 5 detects, on the basis of the demodulated data DD, whether a first test packet TP1 has been received. If, in step SP15, it is judged that a first test packet has not been received, the program proceeds to step SP16 so as to detect whether a second test packet has been received. If, in step SP16, it is judged that a second test packet has not been received, the program returns to SP12. On the other hand, if it is judged in step SP16 that a second test packet has been received, the program proceeds to the next step SP17, in which the count value M corresponding to the number of second test packets received is incremented by "1". Thereafter, the program proceeds to step SP18 in which the CPU 5 provides the buzzer driving signal BS to the buzzer driver 13 for a time period T4 as shown in Figure 4 (c) to cause a warning sound (a short tone) to be generated, indicating that a second test packet TP2 has been received.

At the next step SP19, a judgement is made as to whether the count value N corresponding to the number of receiving operations has reached "99" and, if it has, the program returns to SP2. If this count value N is less than "99", the program proceeds to step SP20, in which it is determined whether the D-switch 16D has been pressed. If the D-switch 16D has been pressed, the program returns to step SP10 while, if the D-switch 16D has not been pressed, the program returns to step SP11.

By repeating the operations of steps SP10 to SP20 as described, the warning sounds (short tone) indicating that a receiving operation has been performed and the warning sounds (short tone) indicating that a second

test packet TP2 has been received are generated alternately, and the respective count values M, representing the number of actual receiving operations effected by the FM receiving circuit 2, and N, representing the number of second test packets received, are displayed by the LCD 12.

When the count value N reaches "99", a shift is made to the preparatory stage for again receiving a first test packet TP1 to be transmitted by the FM transmitting frequency at 88.1 MHz. However, even before the value N reaches "99", if a first test packet TP1 is received, a shift is made to the preparatory stage for receiving the first test packet TP1, since the program returns from step SP15 to step SP2. As shown in Figure 5, if a first test packet is received during an operation for receiving a second test packet TP2, a warning sound indicating that a first test packet has been received is again produced for a time period T1 (one second).

Further, if the D-switch 16D is pressed during the main testing stage, the count values N and M are reset to zero, and the main testing stage is started all over again from the beginning.

If a testing frequency is to be changed, it suffices only to transmit, at a point in time following switching to the preparatory stage as described, a first test packet including frequency data related to the frequency (second testing frequency) by which the next transmission will be made from the testing transmitter. Thus, testing by a second testing frequency may be started, and, similarly, testing by a third testing frequency, by a fourth testing frequency and so on, may proceed sequentially in an efficient manner.

2. Normal receiving mode

A normal receiving mode is started when, after shipment from a factory, the user prepares to receive messages. In the first place, when a power on re-set is effected, for example by changing an internal battery, the CPU 5 executes a fast scanning mode as shown in Figure 3 in steps SP31 to SP35. In step SP31, the receiving frequency of the FM receiving circuit 2 is set to 87.7 MHz. Then, in the next step SP32, an instruction is given to the power supply control circuit 9 to switch the FM receiving circuit 2 from the power saving mode to the power on mode for a time period of about 30 msec to 40 msec in every 0.5 second, thereby causing the FM receiving circuit 2 intermittently to perform the receiving operation.

After each single execution of the receiving operation in step SP32, the program proceeds to the next step SP33, in which the CPU 5 judges, on the basis of the demodulation data DD provided from the decoder 3, whether the count receiving frequency of the FM broadcast frequency at which messages are available, in an attempt to determine the appropriate receiving frequency. If the receiving frequency is not found to be correct in step SP33, the program proceeds to step SP34, in which it is established whether the currently set receiving frequency is 108.0 MHz. If not, the program proceeds to step SF35 and, after up-dating the receiving frequency in step SP35, returns to step SP32. In each step SP35 in this instance, the receiving frequency is initially up-dated sequentially from 87.7 MHz to 107.9 MHz in steps of 0.2 MHz, and is thereafter up-dated sequentially from 87.6 MHz to 108.0 MHz again in steps of 0.2 MHz. Thus, by repeating the operations steps SP32 to SP35 two hundred and four

times, the entire frequency band from 87.6 MHz to 108.0 MHz is scanned.

Supposing that the FM frequency at which the messages are broadcast is 108.0 MHz, then a time period of about 102 seconds (0.5 sec x 204) is necessary for completing the gast scanning mode as described above.

On the other hand, if the receiving frequency is not determined by this fast scanning mode, the program is shifted following step SP34 to a slow scanning mode in which the FM receiving circuit 2 is intermittently operated for a receiving operation at 50 second intervals to scan the entire frequency band of 87.6 MHz to 108.0 MHz to determine the FM frequency at which the messages are being broadcast.

Once the receiving frequency is determined in step SP33, the program proceeds to step SP36 and the FM receiving circuit 2 is then intermittently operated every 1.875 minutes for receiving a message. On receipt of a message, the CPU 5 makes a comparison between the call number included in the transmitted paging data and the personal call number stored in the PROM 17 to judge whether the message in question is directed towards itself.

In the above described embodiment, a change over is made to a testing mode by concurrently pressing the A-switch 16A, the B-switch 16B and the C-switch 16C and, after the change over to this testing mode, the receiving frequency of the FM receiving circuit 2 is instantly initialised to the test starting frequency (88.1 MHz), which is previously defined at the testing transmitter location. Hence, the time needed for processing scanning modes, such as the first scanning mode executed in the normal receiving mode, becomes unnecessary and the time needed for a test operation for

a receiving characteristic is reduced.

Also, if the tests need to be conducted under various frequency conditions, the receiving frequency of a paging receiver may be changed to a desired frequency simply by transmitting a first test packet TP1 including frequency data relating to such desired frequency, whereby the person conducting the test may carry on testing under each new condition without the need for performing any tedious scanning operations.

Further, a warning in the form of a prolonged tone is provided from the buzzer 14 when a first test packet is received, while warnings in the form of respective short tones are alternately provided from the buzzer 14 when a receiving operation is performed and when a second test packet TP2 is received. In addition, the number N of receiving operations effected and the number M of second test packets received are respectively displayed, so that the person conducting the test is able to proceed with the testing of the receiving characteristics effectively simply by recording the contents of the display by the LCD 12 without performing other tedious operations. Furthermore, the transmitting interval T2 for the second test packet TP2 is set to 0.5 second, which is half the transmitting interval T1 for the test packet TP1 to thereby reduce the time required for a single test for a receiving characteristic.

Moreover, the system is switched to a preparatory stage after repeating the receiving operation for second test packets 99 times in the main testing stage, and the FM receiving circuit 2 is forced to enter the power off mode if a first test packet is not received for about two minutes during such a preparatory stage. Therefore, after the completion of a test, the power supply to the

FM receiving circuit 2 is automatically shut off so that power from the internal battery is not wastefully consumed even if the paging receiver is left at a separate location. Thus, the person conducting the test does not have to give any consideration to the power supply of the receiver, even if he or she has left the tested receiver at some other place and has taken up another task. Thereby, no time and labour need be expended in manually turning off the power supply of the paging receiver, testing may proceed smoothly, and a reduction in production costs may also be achieved.

It is also an important advantage of the present paging receiver that the electric current consumed by the FM receiving circuit 2 may be reduced. Normally, the current consumed under the condition where the FM receiving circuit 2 is set to the power on mode reaches up to several tens of mA, the maximum allowable current value, whereas the current consumed under the condition where the FM receiving circuit 2 is set to the power off mode is of the order of several tens of μA. In the embodiment described above, unnecessary current consumption is reduced by automatically switching to the power off mode when a first test packet TP1 has not been received for about two minutes following a change over to the testing mode, and thus a longer life for the internal battery can be expected.

As described above, according to this invention, when an instruction to start a receiving characteristic test is given by operation means, the time previously needed for processing the scanning mode executed in a normal receiving operation is eliminated because the receiving frequency of the receiving circuit is instantly initialised to a previously defined test

starting frequency. The time required for the receiving characteristic test is thus shortened, whereby the receiving characteristic test and any accompanying adjustments may be efficiently carried out. In particular, when the receiving characteristic test is repeated for various changes in environmental conditions, the time and labour required in such tests and accompanying adjustment may be significantly reduced.

CLAIMS

1. A receiver for a paging system, in which a specific frequency for receiving paging data supplied by radio transmission is determined by scanning through a pre-determined frequency band, said receiver comprising a receiving circuit in which a receiving frequency is selectively settable, operation means for generating an instruction to start a receiving characteristic test, and control means responsive to the start instruction to initiate a testing mode by initialising the receiving frequency of said receiving circuit to a previously defined test starting frequency without scanning.

2. A receiver as claimed in claim 1 further comprising storage means for storing identification data for identifying a pre-determined first test packet transmitted at said test starting frequency, said control means being arranged in a preparatory testing stage to detect said first test packet when received by said receiving circuit on the basis of the identification data stored in said storage means.

3. A receiver as claimed in claim 2 in which said control means is arranged to set the receiving frequency of said receiving circuit to a testing frequency determined on the basis of frequency data supplied with said first test packet.

4. A receiver as claimed in claim 3 in which said storage means further stores identification data for identifying a pre-determined second test packet transmitted at said testing frequency, said control means further being arranged in a main testing stage to detect said second test packet after setting the receiving frequency of said receiving circuit to the testing frequency in said preparatory testing stage.

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5. A receiver as claimed in any of claims 2 to 4 in which said control means has an automatic stopping function for stopping receiving by said receiving circuit when said first test packet is not detected within a pre-determined time period following initiation of the testing mode.

6. A receiver as claimed in claim 3 or 4 in which said control means has a receiving operation halt function for halting the receiving by said receiving circuit for the duration of a pre-determined time period after setting the receiving frequency of said receiving circuit to the testing frequency in said prepatory testing stage.

7. A receiver as claimed in claim 4 in which said control means has an automatic return function for returning to said preparatory testing stage by halting the receiving by said receiving circuit for a pre-determined time period on detection of said first test packet during said main testing stage.

8. A receiver as claimed in claim 4 or 6 in which said control means is arranged to co-operate with said receiving circuit whereby said receiving circuit is intermittently operated to receive at a first pre-determined time interval during said preparatory testing stage and at a second pre-determined shorter time interval during said main testing stage.

9. A receiver as claimed in claim 7 in which said control means is arranged to count the number of receiving operations by said receiving circuit and the number of second test packets received and to provide an indication of the result of such counting.

10. A receiver as claimed in any of claims 2 to 8 further comprising warning means operable in response to a signal from said control means to generate a warning

upon the detection of said first test packet.

11. A receiver as claimed in any of claims 4, 7 or to 8 further comprising warning means operable in response to a signal from said control means to generate a warning upon the detection of said second test packet.

12. A receiver according to any preceding claim further comprising display means for displaying information from said control means.

13. A paging receiver for selective calling having a scan mode for determining a specific frequency by scanning through a pre-determined frequency band and receiving selective calling data transmitted through a wireless system at the specific frequency determined by such scan mode, said receiver comprising a receiving circuit capable of voluntarily setting a receiving frequency, operation means for instructing a starter receiving characteristic test, and control means for causing a shift, when a start of test is instructed by said operation means, to a test mode by initialising the receiving frequency of said receiving circuit to a previously defined test starting frequency without executing said scan mode.

14. A receiver for a paging system substantially as herein particularly described with reference to and as illustrated in the accompanying drawings.

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