

[0005] Conventional potential control schemes for potential deviation suppression are costly and time consuming and may fall within one of three conventional methods: a floating-gate transistor method, a back-gate tuning method and a correlated double sampling method. The floating-gate transistor method and the back-gate tuning method are expensive, have high silicon area requirements and are time consuming. The correlated double sampling method disadvantageously generates a large potential swing.

[0006] Thus, what is needed is a quick, inexpensive method for accurately controlling potentials in a potentiostat circuit which at least partially overcomes the drawbacks of present approaches and provides improved silicon real estate requirements, time consumption and reduced potential swing. Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

SUMMARY

[0007] In accordance with an aspect of at least one embodiment of the present invention, a potentiostat control loop circuit is provided. The potentiostat control loop circuit includes a three-electrode potentiostat having a first electrode, a second electrode and a third electrode, where the first electrode is stabilized to a common mode voltage. The circuit also includes a first control amplifier having an output connected to the third electrode of the three-electrode potentiostat and a first input connected to a first potential. The first control amplifier provides a cell voltage to the three-electrode potentiostat, where the cell voltage is a difference between a voltage at

the first electrode of the three-electrode potentiostat and a voltage at a second electrode of the three-electrode potentiostat.

[0008] The potentiostat control loop circuit also includes a first switched capacitor network coupled between a first node and a second input of the first amplifier. The first switched capacitor network includes a first capacitance device having a first electrode connected to the second input of the first control amplifier and a second electrode switchably connectable to either the first node when a first switch of the first switched capacitor network is closed or to the common mode voltage when a second switch of the first switched capacitor network is closed. The second input of the first control amplifier is connected to the first node by a third switch of the first switched capacitor network. The first switched capacitor network is operatively controlled to open the first switch while closing the second and third switches and, alternatively, closing the first switch when opening the second and third switches. The first node is also coupled to the second electrode of the three-electrode potentiostat.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to illustrate various embodiments and to explain various principles and advantages in accordance with a present embodiment.

[0010] FIG. 1, comprising FIGs. 1A and 1B, illustrates circuit diagrams of control loops for conventional potentiostat circuits.

[0011] FIG. 2 illustrates a circuit diagram of a potentiostat control loop using a conventional auto-zero correlated double sampling (CDS) technique.

[0012] FIG. 3 illustrates a circuit diagram of a control loop for a potentiostat circuit in accordance with a first embodiment.

[0013] FIG. 4, comprising FIGs. 4A, 4B and 4C, illustrates a control loop for a potentiostat circuit in accordance with a second embodiment, wherein FIG. 4A illustrates the control loop in accordance with the second embodiment, FIG. 4B illustrates the control loop in accordance with the second embodiment in a clock phase ϕ_1 and FIG. 4C illustrates the control loop in accordance with the second embodiment clock phase ϕ_2 .

[0014] FIG. 5 illustrates a circuit diagram of a control loop for a potentiostat circuit in accordance with a third embodiment.

[0015] FIG. 6 illustrates a graph of simulation results of the operation of the control loop for the potentiostat circuit in accordance with the first embodiment.

CLAIMS

What is claimed is:

1. A potentiostat control loop circuit comprising:

a three-electrode potentiostat having a first electrode, a second electrode and a third electrode, wherein the first electrode is stabilized to a common mode voltage;

a first control amplifier having an output connected to the third electrode of the three-electrode potentiostat and a first input connected to a first potential, the first control amplifier to provide a cell voltage to the three-electrode potentiostat, wherein the cell voltage comprises a difference between a voltage at the first electrode of the three-electrode potentiostat and a voltage at the second electrode of the three-electrode potentiostat; and

a first switched capacitor network coupled between a first node and a second input of the first control amplifier;

wherein the first switched capacitor network comprises a first capacitance device having a first electrode connected to the second input of the first control amplifier and a second electrode switchably connectable to either the first node when a first switch of the first switched capacitor network is closed or to the first potential when a second switch of the first switched capacitor network is closed, the second input of the first control amplifier being connected to the first node by a third switch of the first switched capacitor network and the first switched capacitor network operatively controlled to open the first switch while closing the second and third switches and, alternatively, closing the first switch when opening the second and third switches, wherein the first node is coupled to the second electrode of the three-electrode potentiostat.

2. The potentiostat control loop circuit in accordance with Claim 1 further comprising a switch pair having first ends of first and second switches connected to a second node, a second end of the first switch connected to the third electrode of the three-electrode potentiostat, and a second end of the second switch connected to the second electrode of the three-electrode potentiostat to form a switchable feedback configuration with the three-electrode potentiostat, wherein the switch pair is operatively coupled to the first switched capacitor network such that the first switch of the switch pair is closed and the second switch of the switch pair is open when the first switch of the first switched capacitor network is open and the second and third switches of the first switched capacitor network are closed and, alternatively, the first switch of the switch pair is open and the second switch of the switch pair is closed when the first switch of the first switched capacitor network is closed and the second and third switches of the first switched capacitor network are open.

3. The potentiostat control loop circuit in accordance with Claim 2 wherein the first node is directly connected to the second node.

4. The potentiostat control loop circuit in accordance with Claim 1 wherein the first potential is an input voltage.

5. The potentiostat control loop circuit in accordance with Claim 1 wherein the first potential is a common mode voltage and a second potential coupled to the first node is an input voltage.

6. The potentiostat control loop circuit in accordance with Claim 5 further comprising:

a second control amplifier having a first input connected to the second node and an output coupled to the first node; and

a second switched capacitor network connected to the first input, a second input and the output of the second control amplifier and comprising a second capacitor and a first switch, a second switch and a third switch, the second switched capacitor network operatively coupled to the first switched capacitor network such that the first and third switches of the second switched capacitor network are closed and the second switch of the second switched capacitor network is open when the first switch of the first switched capacitor network is open and the second and third switches of the first switched capacitor network are closed and, alternatively, the first and third switches of the second switched capacitor network are open and the second switch of the second switched capacitor network is closed when the first switch of the first switched capacitor network is closed and the second and third switches of the first switched capacitor network are open.

7. The potentiostat control loop circuit in accordance with Claim 6 further comprising a resistor ladder including a first resistor connected between the input voltage and the first node and a second resistor connected between the first node and the output of the second control amplifier.

8. The potentiostat control loop circuit in accordance with Claim 1 wherein the first capacitance device is a network capacitor.

9. The potentiostat control loop circuit in accordance with Claim 1 wherein the first control amplifier is an operational amplifier and wherein the first input of the first control amplifier is a non-inverted input and the second input of the first control amplifier is an inverted input.

10. The potentiostat control loop circuit in accordance with Claim 6 wherein the second capacitance device is a network capacitor.

11. The potentiostat control loop circuit in accordance with Claim 6 wherein the second control amplifier is an operational amplifier and wherein the first input of the second control amplifier is a non-inverted input and the second input of the first control amplifier is an inverted input.

12. The potentiostat control loop circuit in accordance with Claim 1 wherein the first electrode of the three-electrode potentiostat is a working electrode, a second electrode of the three-electrode potentiostat is a reference electrode and a third electrode of the three-electrode potentiostat is a counter electrode.