

SIGNAL GENERATING APPARATUS AND METHOD, ANALOG-TO-DIGITAL MIXED TEST BOARD, AND TESTER

CROSS-REFERENCE TO RELATED APPLICATION

5 [0001] This application claims priority to Chinese Patent Application No. 202411457686.7, filed on October 18, 2024, and titled “SIGNAL GENERATING APPARATUS AND METHOD, ANALOG-TO-DIGITAL MIXED TEST BOARD, AND TESTER”. The contents of the above identified applications are hereby incorporated herein in their entirety by reference.

TECHNICAL FIELD

[0002] The present invention relates to the field of semiconductor test technologies, and in particular, to a signal generating apparatus and method, an analog-to-digital mixed test board, and a tester.

BACKGROUND

15 [0003] A semiconductor automation test refers to detecting each parameter indicator of a Device Under Test (DUT) by an Automatic Test Equipment (ATE), and removing a defective product to control delivery quality of a semiconductor device. In an analog test, especially in a high-speed analog test, a test signal delivered to the DUT is usually highly required in terms of a harmonic, a signal-to-noise ratio, an amplitude, and a signal frequency. When
20 implementing an IQ (in-phase and quadrature) function, a tester needs to ensure IQ channel synchronization.

[0004] A conventional test signal generating scheme adjusts a sampling clock phase of a DAC (digital-to-analog converter) of IQ channels by changing a frequency of a clock signal output from a clock circuit, so as to synchronize the IQ channels. The test signal is output by adjusting the sampling clock phase of the DAC, which has a complex control logic, a
5 cumbersome operation, and low test efficiency.

[0005] For the issue of the complex control logic, the cumbersome operation, and the low test efficiency for outputting the test signal, no effective solution has been proposed.

SUMMARY

[0006] According to various embodiments of the present invention, a signal generating
10 apparatus and method, an analog-to-digital mixed test board, and a tester are provided.

[0007] In a first aspect, the signal generating apparatus is provided, including an arbitrary waveform generator, a read-write control module, an external clock chip, and a storage apparatus. The external clock chip is configured to output a sampling clock to a digital-to-analog converter, and the sampling clock has a fixed frequency. The read-write control module
15 is connected to the arbitrary waveform generator and the storage apparatus, respectively, and configured to read an original waveform from the storage apparatus according to a received read request instruction and return the read original waveform to the arbitrary waveform generator. The arbitrary waveform generator is configured to perform resampling on the received original waveform to generate a reconstructed waveform that is fitted with the
20 frequency of the sampling clock, and the reconstructed waveform is configured to perform digital-to-analog conversion by the digital-to-analog converter according to the sampling

clock output from the external clock chip.

[0008] In an embodiment, the arbitrary waveform generator further includes a waveform request module and a waveform data processing module. The waveform request module is connected to the read-write control module and the waveform data processing module, respectively, and configured to send the read request instruction to the read-write control module, and send the original waveform returned from the read-write control module to the waveform data processing module. The waveform data processing module is configured to perform resampling on the received original waveform to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

10 [0009] In an embodiment, the arbitrary waveform generator further includes a synchronization control module, which is connected to the waveform data processing module, and configured to cache the reconstructed waveform in an internal cache module and output the reconstructed waveform in the internal cache module after a trigger signal is received.

[0010] In an embodiment, the waveform data processing module further includes a calibrating module and a digital resampling module. The calibrating module is connected to the waveform request module, and configured to perform calibration on the received original waveform and output calibrated waveform data. The digital resampling module is connected to the calibrating module, and configured to perform resampling on the calibrated waveform data to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

[0011] In an embodiment, the calibrating module further includes at least one of a DC (Direct

Current) calibrating module or an AC (Alternating Current) amplitude calibrating module.

[0012] In an embodiment, the digital resampling module further includes an input waveform data cache module, a valid location calculating module, a valid coefficient generating module, a valid data cache module, and a data calculating module. The input waveform data cache
5 module is connected to the calibrating module, the valid location calculating module, and the valid data cache module, respectively, the input waveform data cache module is configured to cache the calibrated waveform data, send a start signal to the valid location calculating module when the quantity of cached data is greater than a specified threshold, read valid data corresponding to a valid location from the cached data according to a received read enable
10 signal, and send the read valid data to the valid data cache module for caching. The valid location calculating module is connected to the valid coefficient generating module, and configured to obtain valid location information by calculation according to a set step and an initial phase after receiving the start signal, send the valid location information to the valid coefficient generating module, and send the read enable signal to the input waveform data
15 cache module. The valid coefficient generating module is connected to the data calculation module and a valid data cache module, respectively, and configured to read a coefficient from a plurality of groups of pre-stored coefficients according to the valid location information, to obtain a valid coefficient and send the valid coefficient to the data calculating module, and send a data-read enable signal to the valid data cache module. The valid data cache module is
20 connected to the data calculating module, and configured to read cached valid data according to the received data-read enable signal and send the cached valid data to the data calculating

module. The data calculating module is configured to perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform.

[0013] In an embodiment, the valid data cache module is configured to store the valid data in
5 a shift manner in parallel into continuous internal cache units. Alternatively, the valid coefficient generating module is configured to read two adjacent groups of coefficients according to integer location information of the valid location information, and perform calculation, according to decimal location information of the valid location information, on the two adjacent groups of coefficients by a linear interpolation algorithm, to obtain the valid
10 coefficient.

[0014] In an embodiment, the data calculating module is configured to perform the convolution calculation according to the received valid coefficient and the received valid data in a following formula:

$$\text{DATA_VALID} = \sum_{k=0}^{15} \text{COE}[k] * \text{DATA_IN}[16 - k]$$

15 DATA_VALID represents a reconstructing point of the reconstructed waveform, COE represents a valid coefficient corresponding to a valid location of the reconstructing point, and DATA_IN represents valid data corresponding to the valid location.

[0015] In an embodiment, the signal generating apparatus further includes a delay module. The arbitrary waveform generator is connected to a corresponding digital-to-analog converter
20 by the delay module, and the arbitrary waveform generator is further configured to

synchronously send valid data to the corresponding digital-to-analog converter according to an associated clock sent by the corresponding digital-to-analog converter.

[0016] In an embodiment, the signal generating apparatus further includes a service decoding module. The service decoding module is connected to a host, the external clock chip, the read-
5 write control module, and the arbitrary waveform generator, respectively, and the service decoding module is configured to perform parameter configuration on the external clock chip and the arbitrary waveform generator according to an instruction sent from the host, and store the original waveform into the storage apparatus by the read-write control module.

[0017] In a second aspect, a signal generating method is provided, including an external clock
10 chip outputting a sampling clock to a digital-to-analog converter, the sampling clock having a fixed frequency, a read-write control module reading an original waveform from a storage apparatus according to a received read request instruction, and returning the read original waveform to an arbitrary waveform generator, and the arbitrary waveform generator performing resampling on the received original waveform to generate a reconstructed
15 waveform that is fitted with the frequency of the sampling clock. The reconstructed waveform is configured to perform digital-to-analog conversion by the digital-to-analog converter according to the sampling clock output from the external clock chip.

[0018] In a third aspect, an analog-to-digital mixed test board is provided, including the signal generating apparatus in the first aspect.

20 [0019] In a fourth aspect, a tester is provided, including a communicating board, a back board, and the analog-to-digital mixed test board in the third aspect.

[0020] Details of one or more embodiments of the present invention are set forth in the accompanying drawings and the description below, so that other features, objects, and advantages of the present invention will be apparent.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0021] To illustrate the technical solutions in the embodiments of the present invention more clearly, the drawings required for describing the embodiments will be described briefly. Apparently, the following described drawings are merely for some embodiments of the present invention, and other drawings can be derived from these drawings by one skilled in the art without any creative effort.

10 [0022] FIG. 1 is a structural block diagram of a signal generating apparatus in an embodiment.

[0023] FIG. 2 is a schematic structural diagram of a signal generation apparatus in an embodiment.

[0024] FIG. 3 is a schematic structural diagram of a waveform data processing module in an embodiment.

15 [0025] FIG. 4 is a schematic principle diagram of digital resampling in an embodiment.

[0026] FIG. 5 is a flowchart of a signal generating method in an embodiment.

DETAILED DESCRIPTION

[0027] To better understand objectives, technical solutions, and advantages of the present invention, the following describes the present invention with reference to the accompanying
20 drawings and embodiments. The specific embodiments described herein are merely used to explain the present invention, and are not intended to limit the present invention.

[0028] Unless otherwise defined, the technical or scientific terms referred to in the disclosure shall have the usual meanings understood by one skilled in the art to which the present disclosure belongs. The terms used in the specification of the present invention are merely intended to describe specific embodiments, and are not intended to limit the present invention.

5 [0029] The “connection” in the following embodiments is understood as “electrical connection”, “communicating connection”, or the like if the connected circuits, modules, units, or the like have transmission of electrical signals or data between each other.

[0030] Words in the present invention such as “one”, “a”, “a kind of”, and/or “the” do not specifically refer to singular, but may also include plural, unless the context clearly indicates
10 another manner. The terms “include”, “contain”, “have” and any variations thereof referred to specify the presence of the stated features, entirety, steps, operations, components, portions or combinations thereof, but does not rule out the possibility of existing or adding one or more other features, entirety, steps, components, portions or combinations thereof. Meanwhile, the term “and/or” used in the specification includes any and all combinations of the items listed.

15 [0031] In an embodiment, referring to FIG. 1, a signal generating apparatus is provided, including an arbitrary waveform generator (AWG) 110, a read-write control module 120, an external clock chip 130, and a storage apparatus 140. The read-write control module 120 is connected to the AWG 110 and the storage apparatus 140, respectively. Furthermore, the signal generating apparatus may further include a digital-to-analog converter (DAC) 150
20 connected to the AWG 110. The external clock chip 130 is configured to output a sampling clock to the DAC, and the sampling clock has a fixed frequency. The read-write control

module 120 is configured to read an original waveform from the storage apparatus 140 according to a received read request instruction and return the read original waveform to the AWG 110. The AWG 110 is configured to perform resampling on the received original waveform to generate a reconstructed waveform that is fitted with the frequency of the sampling clock, and the reconstructed waveform is configured to perform digital-to-analog conversion by the DAC according to the sampling clock output from the external clock chip.

[0032] The AWG 110 generates the reconstructed waveform fitted with the frequency of the sampling clock, which may refer to a sampling rate of the reconstructed waveform being the same as the frequency of the sampling clock, or an error between the sampling rate of the reconstructed waveform and the frequency of the sampled clock being within an allowed range. The external clock chip 130 may include a Phase Locked Loop (PLL) clock chip, and the storage apparatus 140 may include a Double Data Rate (DDR) storage apparatus, which includes a DDR4 RAM. The quantity of the AWG 110 may be one or more, and the quantity of the DAC 150 may be in a one-to-one correspondence with that of the AWG 110. For example, for IQ channels of the tester, one AWG 110 and one DAC 150 may be disposed, respectively. After the read-write control module 120 reads the original waveform according to the received read request instruction, the read-write control module 120 returns the read original waveform to the AWG 110 of a corresponding channel. After the AWG 110 receives the original waveform, the AWG 110 may perform Direct Current (DC) calibration, Alternating Current (AC) calibration, resampling, or the like, generate the reconstructed waveform, and send the reconstructed waveform to a corresponding DAC 150 for performing

digital-to-analog conversion, to obtain an analog waveform output signal, which is configured to test a DUT such as a semiconductor chip. To meet a requirement of the DAC 150, a frequency of the original waveform arbitrarily disposed by the user may be less than or equal to the frequency of the sampling clock output from the external clock chip 130.

5 [0033] Furthermore, referring to FIG. 2, the signal generating apparatus may further include a service decoding module 160. The service decoding module 160 may be connected to a host, the external clock chip 130, the read-write control module 120, and the AWG 110, respectively. The service decoding module 160 may perform parameter configuration on the external clock chip 130 and the AWG 110 according to an instruction sent from the host, and store the
10 original waveform into the storage apparatus 140 by the read-write control module 120. The read-write control module 120 may be connected to the storage apparatus 140 by an Avalon interface.

[0034] Specifically, the AWG 110, the read-write control module 120, and the service decoding module 160 may be disposed in a Field-Programmable Gate Array (FPGA), and the
15 external clock chip 130, the storage apparatus 140, and the DAC 150 may be located outside the FPGA. A port PLL_CTRL of the service decoding module 160 may be connected to the external clock chip 130 by a Serial Peripheral Interface (SPI), and configure parameters of the external clock chip 130, so that the external clock chip 130 outputs the sampling clock at the fixed frequency to the DAC 150. The external clock chip 130 may be configured to output
20 the sampling clock at a maximum allowed frequency (e.g., 400 MHz), or may be configured to output the sampling clock at another frequency. A port DDR_RQE of the service decoding

module 160 may be connected to the read-write control module 120, and read-write control of the waveform may be implemented on the storage apparatus 140 by the read-write control module 120. A port AWG_CTRL of the service decoding module 160 may be connected to the AWG 110, and deliver a control signal parameter to perform waveform resampling control
5 on the AWG 110.

[0035] After the signal generating apparatus is powered on, the service decoding module 160 may automatically configure, by the SPI, the external clock chip 130 to output the sampling clock at the fixed frequency, and the host may write the original waveform into the storage apparatus 140 by the service decoding module 160 and the read-write control module 120.
10 The host may further deliver the control signal parameter to the AWG 110 by the service decoding module 160. The AWG 110 may send the read request instruction to the read-write control module 120 according to the received control signal parameter, and perform resampling processing on the original waveform returned from the read-write control module 120 to generate the reconstructed waveform that is fitted with the frequency of the sampling
15 clock.

[0036] Referring to FIG. 2, two DAC chips of the IQ channels may be same DAC chips, and the sampling clock of the DAC chips may be set to a fixed maximum sampling clock (400 MHz). A sampling rate of the original waveform in the storage apparatus 140 may be randomly set by the user. However, the DAC chips may be in operation by using the fixed
20 maximum sampling clock. Therefore, the original waveform may be resampled by the AWG 110, in a case that waveform information (amplitude and frequency) is not changed, the

original waveform at any sampling rate stored in the storage apparatus 140 may be resampled to the fixed maximum sampling clock, so that the sampling rate of the obtained reconstructed waveform may be the same as the frequency of the sampling clock of the DAC chips. Meanwhile, in a resampling process, an initial phase of the reconstructed waveform generated
5 by resampling may be changed by setting the initial phase. The generated reconstruction waveform may be output to the DAC chips to implement any sampling rate and any phase adjustment of the IQ channels. An IQ function may be implemented by using two common DAC chips, and a non-IQ function may also be implemented. A frequency of the sampling clock may not need to be adjusted by the external clock chip 130, thereby simplifying an
10 operation and improving test efficiency.

[0037] In an embodiment, the AWG 100 may further include a waveform request module 112 and a waveform data processing module 114. The waveform request module 112 may be connected the read-write control module 120 and the waveform data processing module 114, respectively, and configured to send the read request instruction to the read-write control
15 module 120, and send the original waveform returned from the read-write control module 120 to the waveform data processing module 114. The waveform data processing module 114 is configured to perform resampling on the received original waveform to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

[0038] The waveform request module 112 may include a waveform request unit 1122, a
20 Random Access Memory (RAM) storage unit 1124, and a data selecting unit 1126. The waveform request unit 1122 may be connected to the read-write control module 120, the RAM

storage unit 1124, and the data selecting unit 1126, respectively, and the data selecting unit 1126 may be connected to the RAM storage unit 1124 and the waveform data processing module 114, respectively. Furthermore, the waveform request unit 1122 and the data selecting unit 1126 may be connected to the service decoding module 160, respectively.

5 [0039] The waveform request unit 1122 may initiate the read request instruction to the read-write control module 120 according to the control signal parameter (including a PRE_START instruction, an AWG_CTRL_SIGNAL instruction, or the like) delivered by the service decoding module 160, to request to read a corresponding original waveform. The AWG_CTRL_SIGNAL instruction may include information such as a waveform length, a
10 start address of the original waveform in the storage apparatus 140, or the quantity of repeating sending times of the waveform. When the PRE_START instruction is 1, an original waveform of an I channel may be requested from the read-write control module 120. When the PRE_START instruction is 2, an original waveform of a Q channel may be requested from the read-write control module 120. When the PRE_START instruction is 3, original
15 waveforms of the I channel and the Q channel may be requested simultaneously from the read-write control module 120. After the read-write control module 120 responds to the read request instruction, the original waveforms of the I channel and the Q channel may be correspondingly output to the waveform requesting unit 1122 according to requested channel data information. After receiving the original waveform, the waveform requesting unit 1122
20 may determine, according to the waveform length, whether to write the original waveform into the RAM storage unit 1124. If the waveform length is less than a preset threshold length

(e.g., 1024), the waveform requesting unit 1122 may write the original waveform into the RAM storage unit 1124; otherwise, the waveform requesting unit 1122 may directly output the original waveform to the data selecting unit 1126. The data selecting unit 1126 may determine a source of the original waveform according to a waveform length parameter (such
5 as a AWG_Digital_CTRL_SIGNAL instruction) delivered by the service decoding module 160. If the waveform length is less than a preset threshold length, the data selecting unit 1126 may allow the RAM storage unit 1124 to output the original waveform; otherwise, the data selecting unit 1126 may allow the waveform requesting unit 1122 to directly output the original waveform. The data selecting unit 1126 may send the original waveform to the
10 waveform data processing module 114 for resampling processing.

[0040] Since the length of the original waveform may be very small, in a case that the length of the original waveform is very small, DDR may have a low bandwidth utilization and be insufficient to support continuous output of the waveform. In this case, the original waveform may need to be stored in the RAM storage unit 1124 to control output of the original waveform
15 from the RAM storage unit 1124, so as to reduce impact of bandwidth sacrifice of the DDR on small data. The RAM storage unit 1124 may support a repeating read operation of the waveform, support continuous waveform output, and further support stopping a read operation. When the length of the waveform is small, the original waveform may be stored in the RAM storage unit 1124, and continuous output of the waveform may be implemented by
20 using the RAM storage unit 1124.

[0041] In an embodiment, referring to FIG. 2, the AWG 100 may further include a

synchronization control module 116, which is connected to the waveform data processing module 114, and configured to cache the reconstructed waveform in an internal cache module and output the reconstructed waveform in the internal cache module after a trigger signal is received. Specifically, the synchronization control module 116 may further be connected to
5 the service decoding module 160, and the synchronization control module 116 may cache the received reconstructed waveform in an internal First Input First Output (FIFO) cache. After receiving the trigger signal TRIG sent from the service decoding module 160, the synchronization control module 116 may output the reconstructed waveform in the FIFO cache to the DAC 150. In addition, taking that a tester includes the IQ channels as an example,
10 synchronization control may be performed by synchronization control modules 116 in the IQ channels, and reconstruction waveforms of the two channels may be synchronously sent to two DAC chips of the IQ channels, respectively.

[0042] A specific structure of the waveform data processing module 114 may not be unique. The waveform data processing module 114 may include a calibrating module and a digital
15 resampling module. The calibrating module may be connected to the waveform request module 112, and configured to perform calibration on the received original waveform and output calibrated waveform data. The digital resampling module may be connected to the calibrating module, and configured to perform resampling on the calibrated waveform data to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

20 [0043] Referring to FIG. 3, the calibrating module may specifically include at least one of a Direct Current (DC) calibrating module 41 or an Alternating Current (AC) amplitude

calibrating module 42. Taking that the calibrating module includes the DC calibrating module 41 and the AC amplitude calibrating module 42 as an example, both the DC calibrating module 41 and the AC amplitude calibrating module 42 may be connected to the service decoding module 160, the DC calibrating module 41 may be connected to the data selecting unit 1126 in the waveform request module 112, and the AC amplitude calibrating module 42 may be connected to the DC calibrating module 41 and the digital resampling module. The DC calibrating module 41 may perform DC calibration on the received original waveform according to a DC calibration coefficient delivered by the service decoding module 160, and send the calibrated waveform to the AC amplitude calibrating module 42, so as to ensure that amplitude precision of channel data meets an indicator requirement. Since the IQ channels require relatively high flatness of the AC, the AC amplitude calibrating module 42 may further perform AC amplitude calibration on the waveform after the DC calibration according to an AC calibration coefficient delivered by the service decoding module 160, so as to ensure that the amplitude precision of the channel data meets the indicator requirement. The AC amplitude calibrating module 42 may send the waveform after the AC amplitude calibration to the digital resampling module.

[0044] The storage apparatus 140 may store the original waveform whose frequency is set by the host (the frequency is variable, e.g., 100MHz, i.e., the original waveform whose frequency is set by the user at any frequency), and the external clock chip 130 may be set at a fixed maximum sampling clock frequency. A function of the digital resampling module may be to resample the original waveform to the reconstructed waveform at the fixed maximum

sampling clock frequency (400M) (both the waveform data and the sampling frequency may be converted, and based on the maximum sampling clock frequency, the original waveform may be converted to the reconstructed waveform corresponding to the maximum sampling clock frequency).

5 [0045] A principle of resampling is that a SINC function is used to perform waveform recovery for a continuous signal. Since the AWG 110 resamples the original waveform at any frequency to the waveform at the fixed maximum sampling frequency, an actual function may be summarized as an interpolation of multiple of any decimal. For a known continuous waveform $x(n)$, data resampling recovery may be performed by using the SINC function to
10 recover $x(n)$ to $x(t)$ at any time. By using 8 forward points and 8 backward points of a location of a valid point to be recovered, an actual value of the recovered point may be obtained after a convolution operation of 16 pieces of data of the 8 forward points and 8 backward points and 16 continuous SINC coefficients is performed.

[0046] To recover an ideal SINC function, countless sets of coefficients may be required to
15 perform the operation in theory. Apparently, it is not feasible. Therefore, a model of the SINC function may be selected and divided into 1024 groups of coefficients, each of which includes 16 coefficients stored in a ROM, and a valid coefficient may be read from the ROM according to the valid location information. Since infinite multiple groups of coefficients cannot be stored, for higher precision, the stored coefficients may not be directly used when calculating
20 the valid coefficient, but be considered as continuous coefficients between each group of coefficients, and the valid coefficient of any point may be obtained by using a linear weighting

algorithm.

[0047] Based on this, referring to FIG. 3, the digital resampling module may include an input waveform data cache module 43, a valid location calculating module 44, a valid coefficient generating module 45, a valid data cache module 46, and a data calculating module 47. The input waveform data cache module 43 may be connected to the calibrating module, the valid location calculating module 44, and the valid data cache module 46, respectively. The valid location calculating module 44 may be connected to the valid coefficient generating module 45, the valid coefficient generating module 45 may be connected to the data calculating module 47 and the valid data cache module 46, respectively, and the valid data cache module 46 may be connected to the data calculating module 47.

[0048] Specifically, the input waveform data cache module 43 may be connected to the AC amplitude calibrating module 42 in the calibrating module, and configured to cache the calibrated waveform data, send a start signal SINC_START to the valid location calculating module 44 when the quantity of cached data is greater than a specified threshold quantity, read valid data corresponding to a valid location from the cached data according to a received read enable signal, and send the read valid data to the valid data cache module 46 for caching. The valid location calculating module 44 is configured to obtain valid location information by calculation according to a set step and an initial phase after receiving the start signal SINC_START, send the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43. The valid coefficient generating module 45 is configured to read a coefficient from a plurality of groups

of pre-stored coefficients according to the valid location information, to obtain a valid coefficient and send the valid coefficient to the data calculating module 47, and send a data-read enable signal to the valid data cache module 46. The valid data cache module 46 is configured to read cached valid data according to the received data-read enable signal and
 5 send the cached valid data to the data calculating module 47. The data calculating module 47 is configured to perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform. A convolution formula may be as follows:

$$\text{DATA_VALID} = \sum_{k=0}^{15} \text{COE}[k] * \text{DATA_IN}[16 - k]$$

10 DATA_VALID represents a reconstructed point of the reconstructed waveform, COE represents a valid coefficient (16 valid coefficients in total) corresponding to a valid location of the reconstructed point, and DATA_IN represents valid data (16 points, including 8 forward points and 8 backward points of the valid location) corresponding to the valid location. After 16 times of multiplication and accumulation of the valid coefficient and the original waveform
 15 are performed, a corresponding reconstructed point of the reconstructed waveform may be obtained.

[0049] A value of the specified threshold quantity may not be unique and may be set as required. The service decoding module 160 may be connected to the valid location calculating module 44, and configure the set step STEP and the initial phase PHASE. The digital
 20 resampling module may resample an initial waveform at a variable sampling frequency to the

reconstructed waveform at the fixed maximum sampling frequency. In addition, since the digital resampling module performs digital resampling, phase adjustment of an output waveform may be further implemented, and adjustment precision may be up to 1ps.

[0050] Specifically, after the input waveform data cache module 43 receives the calibrated waveform data output from the AC amplitude calibrating module 42, the calibrated waveform data may be cached in the internal cache unit (e.g., the FIFO). When the quantity of cached data is greater than the specified threshold quantity (e.g., 16), the input waveform data cache module 43 may send the start signal SINC_START to the valid location calculating module 44. After receiving the start signal SINC_START, the valid location calculating module 44 may start to operate, and perform valid location calculating according to the step STEP and the initial phase PHASE that are sent by the service decoding module 160. The valid location may be understood as a location of a reconstructed waveform point, and the calculated valid location may include a 16-bit integer and a 48-bit decimal. An initial location of the reconstructed waveform may be determined by the initial phase PHASE, and the initial location may refer to a valid location of a first point of the reconstructed waveform. A relationship between the location of the reconstructed waveform point and a location of an original waveform point may be as follows: the location of the reconstructed waveform point = (the location of the original waveform point - 1) * STEP + 1 + PHASE. The location of the original waveform point may be a location of a calibrated waveform data point, and DC calibration and AC amplitude calibration may not change the location of the original waveform point.

[0051] The step STEP = a sampling rate (the sampling rate of the original waveform) set by the user / the fixed maximum sampling rate (the frequency of the sampling clock). Since the sampling rate set by the user is less than or equal to the fixed maximum sampling rate, a value of the STEP may be less than or equal to 1, which may be understood as an interpolation operation with any multiple. The step STEP may include the 16-bit integer and the 48-bit decimal. Since the fixed maximum sampling rate is set as 400 MHz, and a 48-bit decimal may be supported to uHz, the sampling rate of resampling may have a precision of uHz. Since the AWG 110 outputs at a fixed sampling rate of 400 MHz, uHz adjustment may be implemented to achieve sampling rate resolution. Assuming that $A = 400 \text{ MHz} = 400 \times 2^{10} \times 2^{10} \text{ Hz}$ and $B = 1 \text{ uHz} = (1/2^{10} \times 2^{10}) \text{ Hz}$, $A/B = 400 \times 2^{10} \times 2^{10} \text{ Hz} / (1/2^{10} \times 2^{10}) \text{ Hz} = 400 \times 2^{40} = 49 \text{ bit}$. Since an SINC algorithm divides the coefficient into 1024 pieces, the minimum location information may need $400 \times 2^{40} / 1024 \text{ bit} = 39 \text{ bit}$. In the present invention, 48 bit may be selected. The initial phase PHASE = the quantity of the points in a waveform period / $(360^\circ / \text{a phase of the reconstructed waveform})$, and an output result may be represented by the 16-bit integer and the 48-bit decimal, so that ps-level phase adjustment may be performed.

[0052] After obtaining the valid location information according to the set step STEP and the initial phase PHASE, the valid location calculating module 44 may output the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43 according to the obtained valid location. The input waveform data cache module 43 may read, according to the read enable signal sent by the valid location calculating module 44, one piece of data, and send the piece of data to the valid

data cache module 46. In this case, the piece of data stored in the valid data cache module 46 may be valid data of the valid location. After the valid coefficient generating module 45 calculates the valid coefficient of the valid location, the valid data cache module 46 may read the valid data and send the valid data to the data calculating module 47 for calculation.

5 [0053] The valid coefficient generating module 45 may store multiple groups (e.g., 1024 groups) of coefficients (16 coefficients in each group) in an internal ROM (read-only memory) unit in advance. After receiving the valid location information, the valid coefficient generating module 45 may read two adjacent groups of coefficients according to integer location information of the valid location information, and calculate the two adjacent groups of
10 coefficients by using a linear interpolation algorithm according to the decimal location information of the valid location information to obtain the valid coefficient.

[0054] Specifically, the valid coefficient generating module 45 may read a pre-stored coefficient from the ROM unit according to the valid location information. Since there are 1024 groups of pre-stored coefficients and 48-bit decimal precision cannot be met, in this case,
15 the valid coefficient generating module 45 may read two adjacent groups of coefficients (16 coefficients in a group) according to the integer location information of the valid location information, and calculate the two groups of coefficients according to the decimal location information of the valid location information by the linear interpolation algorithm: $Y_coe[n] = COE1[n]*tim_valid + COE2[n]*(1-tim_valid)$, n is set to 0-15 to obtain the most accurate
20 valid coefficient (16 coefficients). COE1 represents a first group of coefficients in the two adjacent groups of coefficients that are read out, COE2 represents a second group of

coefficients (both the first group of coefficients and the second group of coefficients include 16 coefficients) in two adjacent groups of coefficients that are read out, `tim_valid` represents the decimal location information of the valid location information, and `y_coe` represents the valid coefficient (16 coefficients) of the decimal position in actual valid location information
5 that is obtained by the linear interpolation.

[0055] The valid data cache module 46 may store the valid data in a shift manner in parallel into continuous internal cache units (e.g., FIFO). Specifically, the valid data cache module 46 may store the valid data in 16 FIFOs in a shift manner in parallel. A specific representation of the parallel storage may be as follows: latest input data may be stored in FIFO1, original data
10 in the FIFO1 may be stored in FIFO2, and original data in the FIFO2 may be stored in FIFO3, ..., i.e., 16 consecutive pieces of data may be stored in the 16 FIFOs.

[0056] After generating a valid coefficient, the valid coefficient generating module 45 may output the valid coefficient to the data calculating module 47, and simultaneously send a data-read enable signal to the valid data cache module 46. The valid data cache module 46 may
15 simultaneously read 16 pieces of valid data in the 16 FIFOs according to the data-read enable signal, and output the 16 pieces of valid data to the data calculating module 47. The data calculating module 47 may perform 16-order convolution calculation according to the valid coefficient output from the valid coefficient generating module 45 and the valid data output from the valid data cache module 46, to obtain the reconstructed waveform after resampling
20 and output the reconstructed waveform to the subsequent synchronization control module 116.

[0057] The following is an example for description. It is assumed that condition 1: the

sampling rate (the frequency of the original waveform) is set by the user to 202MHz, condition 2: a phase of the reconstructed waveform is set to 3.6°, and condition 3: a waveform file has 100 points, which indicates two periods. In this case, the step STEP = the sampling rate set by the user / the fixed maximum sampling rate = 202 / 400 = 0.505, the initial phase

5 PHASE = the quantity of the points in a waveform period / (360° / the phase of the reconstructed waveform) = (100 / 2) / (360° / 3.6°) = 0.5. Referring to FIG. 4, in the reconstructed waveform, the valid location of a first point may be determined according to the initial phase PHASE, and the reconstructed waveform point may be corresponding to the valid location in the original waveform. The relationship between the location of the

10 reconstructed waveform point and the location of the original waveform point may be as follows: the location of the reconstructed waveform point = (the location of the original waveform point - 1) * STEP + 1 + PHASE = (the location of the original waveform point - 1) * 0.505 + 1 + 0.5, such as 1----1.500, 2----2.005, 3----2.510, and 4-----3.015. Referring to FIG. 4, it is described that the effects of the frequency set by the user, the quantity of waveform

15 points, and the initial phase on resampling, and a relationship between the frequency set by the user, the quantity of waveform points, the initial phase and the valid location.

[0058] In an embodiment, the signal generating apparatus may further include a delay module. The AWG 110 may be connected to a corresponding DAC 150 by the delay module, and the AWG 110 is further configured to synchronously send the valid data to the corresponding

20 digital-to-analog converter according to an associated clock sent by the corresponding DAC 150. Referring to FIG. 2, the delay module may specifically include an IDELAY unit and an

ODELAY unit. Since different traces cause different delays, the IDELAY unit and the ODELAY unit are used to adjust the delay of the transmission of the reconstructed waveform, so that the DAC chip may meet establishment of maintenance time. The synchronization control module 116 in the AWG 110 may be connected to the corresponding DAC 150 by the
5 delay module, and the synchronization control module 116 may be connected to the delay module by a Low-Voltage Differential Signaling (LVDS) interface. The DAC 150 may output the associated clock data_clk to the synchronization control module 116, and the synchronization control module 116 may output the reconstructed waveform according to the associated clock data_clk.

10 [0059] Similarly, taking that the tester includes IQ channels as an example, both the two DAC chips of the two channels may send the associated clock data_clk. Since the sampling clock input to the two DAC chips is of the same source and the same frequency, one sampling clock may be used as a common sampling clock of the two DAC chips. The two DAC chips may output the associated clock data_clk to synchronization control modules 116, respectively,
15 and the synchronization control modules 116 may output the reconstructed waveform to the DAC chips according to the associated clock data_clk, respectively.

[0060] To ensure data synchronization, after receiving a trigger signal TRIG, the synchronization control module 116 may first convert the trigger signal TRIG into a clock domain of the associated clock data_clk of an I-channel DAC chip, and then determine,
20 according to an operating mode delivered from the service decoding module 160, whether the operating mode is an IQ mode. If yes, it may be determined that as long as the trigger signal

TRIG of one channel is pulled up, the synchronization control modules 116 of the two channels are controlled to read data from the FIFO at the same time and output data according to the associated clock data_clk of the I-channel DAC chip as a clock. In this case, synchronous output of data of the IQ channels may be achieved. If no, the synchronization control modules 116 of the IQ channels may control the output of the IQ channels according to received TRIG signals, respectively.

[0061] Referring to FIG. 2 and FIG. 3, the following describes a complete processing of the original waveform: after the signal generating apparatus is powered on, the host may be in communication with the service decoding module 160, write the original waveform into the storage apparatus 140 by the service decoding module 160, configure the external clock chip 130 to output the sampling clock with the fixed frequency, and deliver the control signal parameter to the AWG 110 for parameter configuration. The control signal parameter may specifically include a control signal parameter of the waveform request unit 1122, a waveform length parameter of the data selecting unit 1126, a DC calibrating parameter of the DC calibrating module 41, an AC calibrating parameter of the AC amplitude calibrating module 42, the step and the initial phase of the valid location calculating module 44, or the like.

[0062] The waveform request unit 1122 may send a read request instruction to the read-write control module 120 according to the configured control signal parameter to request to read the original waveform. After receiving the original waveform, the waveform request unit 1122 may determine, according to the waveform length, whether to write the original waveform into the RAM storage unit 1124. If the waveform length is less than the preset threshold length,

the waveform request unit 1122 may write the original waveform into the RAM storage unit 1124. Otherwise, the waveform request unit 1122 may directly output the original waveform to the data selecting unit 1126. The data selecting unit 1126 may determine the source of the original waveform according to the waveform length parameter delivered by the service
5 decoding module 160, acquire the original waveform from the RAM storage unit 1124 or the waveform request unit 1122, and send the original waveform to the waveform data processing module 114 for resampling processing.

[0063] In the waveform data processing module 114, the DC calibrating module 41 and the AC amplitude calibrating module 42 may sequentially perform DC calibration and AC
10 amplitude calibration on the original waveform according to the configured DC calibrating coefficient and AC calibrating coefficient, and then send the calibrated waveform to the input waveform data cache module 43 for caching. The input waveform data cache module 43 may send the start signal SINC_START to the valid location calculating module 44 when the quantity of cached data is greater than the specified threshold quantity. After receiving the
15 start signal SINC_START, the valid location calculating module 44 may calculate the valid location information according to a configured step and the initial phase, send the valid location information to the valid coefficient generating module 45, and send the read enable signal to the input waveform data cache module 43. The input waveform data cache module 43 may read, according to the received read enable signal, the valid data corresponding to the
20 valid location from the cached data, and send the read valid data to the valid data cache module 46 for caching. The valid coefficient generating module 45 may read coefficients from

the multiple groups of pre-stored coefficients according to the valid location information, to obtain the valid coefficient and send the valid coefficient to the data calculating module 47, and send the data-read enable signal to the valid data cache module 46. The valid data cache module 46 may read the cached valid data according to the received data-read enable signal,
5 and send the cached valid data to the data calculating module 47. The data calculating module 47 may perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed waveform.

[0064] The reconstructed waveform obtained by the data calculation module 47 may be sent to the synchronization control module 116 for caching. After receiving the trigger signal TRIG
10 delivered by the service decoding module 160, the synchronization control module 116 may send, taking the associated clock data_clk of the DAC chip as a clock, the cached reconstructed waveform to the DAC chip by the delay module. The DAC chip may perform digital-to-analog conversion on the received reconstructed waveform according to the sampling clock output from the external clock chip 130, to obtain an analog waveform signal,
15 and output the analog waveform signal to the DUT for testing.

[0065] In an embodiment, referring to FIG. 5, a signal generating method is provided, including step 110 to step 130.

[0066] Step 110 includes an external clock chip outputting a sampling clock to a digital-to-analog converter, and the sampling clock having a fixed frequency.

20 [0067] Step 120 includes a read-write control module reading an original waveform from a storage apparatus according to a received read request instruction, and returning the read

original waveform to an arbitrary waveform generator.

[0068] Step 130 includes the arbitrary waveform generator performing resampling on the received original waveform to generate a reconstructed waveform that is fitted with the frequency of the sampling clock. The reconstructed waveform is configured to perform
5 digital-to-analog conversion by the digital-to-analog converter according to the sampling clock output from the external clock chip.

[0069] It may be understood that a specific implementation of the foregoing signal generating method is described in detail in the foregoing signal generating apparatus, and details are not described herein again.

10 [0070] In an embodiment, an analog-to-digital mixed test board is provided, including the signal generating apparatus.

[0071] In an embodiment, a tester is provided, including a communicating board, a back board, and the analog-to-digital mixed test board. The communicating board is connected to the analog-to-digital mixed test board by the back board. In addition, the tester may further
15 include a host that is in communication with the communicating board. The host may be but is not limited to various personal computers, laptops, smartphones, tablets, and portable wearable devices. The portable wearable devices may include a smart watch, a smart band, a headset, or the like.

[0072] The foregoing signal generating apparatus and method, the analog-to-digital mixed
20 test board, and the tester have the following advantages.

[0073] 1. In the present invention, the sampling clock of the DAC chip with fixed frequency

may be used. After being powered on and initialized, the external clock chip may not need to be repeatedly configured, thereby reducing locking time of the clock chip generated by changing the sampling clock, and improving test efficiency.

[0074] 2. In the present invention, the sampling clock of the DAC chip with fixed frequency
5 may be used, and a resampling operation may be performed by a digital domain algorithm to implement design of any sampling rate, so that an adjustment of sampling rate with a resolution of uHz may be implemented. This indicator requirement is an indicator requirement that is difficult to be implemented in a conventional manner of adjusting the sampling rate by a clock chip.

10 [0075] 3. In the present invention, both an IQ function and a non-IQ function may be implemented, and the use may be more flexible and convenient, thereby improving use efficiency of the apparatus.

[0076] 4. A control manner of the present invention may facilitate extension, multiplexing, and transplantation of program channels, and may be directly configured in another project.
15 For program updates, a channel may need to be added or reduced, thereby facilitating program code maintenance.

[0077] All the technical features in the foregoing embodiments may be combined randomly. To make the description brief, all possible combinations of the technical features in the foregoing embodiments are not described. However, as long as there is no contradiction
20 between the combinations of the technical features, it should be considered as the scope described in this specification.

[0078] The foregoing embodiments represent only several implementation manners of the present invention, and descriptions thereof are relatively specific and detailed, but may not be construed as a limitation on the scope of the present invention. It should be noted that one skilled in the art may make some modifications and improvements without departing from the concept of the present invention, which are within the protection scope of the present invention. Therefore, the protection scope of the present invention shall be subject to the appended claims.

CLAIMS

What is claimed is:

1. A signal generating apparatus, characterized by comprising an arbitrary waveform generator, a read-write control module, an external clock chip, and a storage apparatus,
5 wherein

the external clock chip is configured to output a sampling clock to a digital-to-analog converter, and the sampling clock has a fixed frequency;

the read-write control module is connected to the arbitrary waveform generator and the storage apparatus, respectively, and configured to read an original waveform from the storage
10 apparatus according to a received read request instruction and return the read original waveform to the arbitrary waveform generator; and

the arbitrary waveform generator is configured to perform resampling on the received original waveform to generate a reconstructed waveform that is fitted with the frequency of the sampling clock, and the reconstructed waveform is configured to perform digital-to-
15 analog conversion by the digital-to-analog converter according to the sampling clock output from the external clock chip.

2. The signal generating apparatus of claim 1, wherein the arbitrary waveform generator further comprises a waveform request module and a waveform data processing module,
20 wherein

the waveform request module is connected to the read-write control module and the

waveform data processing module, respectively, and configured to send the read request instruction to the read-write control module, and send the original waveform returned from the read-write control module to the waveform data processing module; and

the waveform data processing module is configured to perform resampling on the
5 received original waveform to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

3. The signal generating apparatus of claim 2, wherein the arbitrary waveform generator further comprises a synchronization control module, which is connected to the waveform data
10 processing module, and configured to cache the reconstructed waveform in an internal cache module and output the reconstructed waveform in the internal cache module after a trigger signal is received.

4. The signal generating apparatus of claim 2, wherein the waveform data processing module
15 further comprises a calibrating module and a digital resampling module,

the calibrating module is connected to the waveform request module, and configured to perform calibration on the received original waveform and output calibrated waveform data; and

the digital resampling module is connected to the calibrating module, and configured to
20 perform resampling on the calibrated waveform data to generate the reconstructed waveform that is fitted with the frequency of the sampling clock.

5. The signal generating apparatus of claim 4, wherein the calibrating module further comprises at least one of a Direct Current calibrating module or an Alternating Current amplitude calibrating module.

5

6. The signal generating apparatus of claim 4, wherein the digital resampling module further comprises an input waveform data cache module, a valid location calculating module, a valid coefficient generating module, a valid data cache module, and a data calculating module,

the input waveform data cache module is connected to the calibrating module, the valid
10 location calculating module, and the valid data cache module, respectively, the input waveform data cache module is configured to cache the calibrated waveform data, send a start signal to the valid location calculating module when the quantity of cached data is greater than a specified threshold, read valid data corresponding to a valid location from the cached data according to a received read enable signal, and send the read valid data to the valid data
15 cache module for caching;

the valid location calculating module is connected to the valid coefficient generating module, and configured to obtain valid location information by calculation according to a set step and an initial phase after receiving the start signal, send the valid location information to the valid coefficient generating module, and send the read enable signal to the input waveform
20 data cache module;

the valid coefficient generating module is connected to the data calculation module and

a valid data cache module, respectively, and configured to read a coefficient from a plurality of groups of pre-stored coefficients according to the valid location information, to obtain a valid coefficient and send the valid coefficient to the data calculating module, and send a data-read enable signal to the valid data cache module;

5 the valid data cache module is connected to the data calculating module, and configured to read cached valid data according to the received data-read enable signal and send the cached valid data to the data calculating module; and

 the data calculating module is configured to perform convolution calculation according to the received valid coefficient and the received valid data to obtain the reconstructed
10 waveform.

7. The signal generating apparatus of claim 6, wherein the valid data cache module is configured to store the valid data in a shift manner in parallel into continuous internal cache units, optionally wherein

15 the valid coefficient generating module is configured to read two adjacent groups of coefficients according to integer location information of the valid location information, and perform calculation, according to decimal location information of the valid location information, on the two adjacent groups of coefficients by a linear interpolation algorithm, to obtain the valid coefficient.

20

8. The signal generating apparatus of claim 6, wherein the data calculating module is

configured to perform the convolution calculation according to the received valid coefficient and the received valid data in a following formula:

$$\text{DATA_VALID} = \sum_{k=0}^{15} \text{COE}[k] * \text{DATA_IN}[16 - k]$$

wherein DATA_VALID represents a reconstructing point of the reconstructed waveform,

5 COE represents a valid coefficient corresponding to a valid location of the reconstructing point, and DATA_IN represents valid data corresponding to the valid location.

9. The signal generating apparatus of any one of claims 1 to 8, further comprising a delay module, wherein the arbitrary waveform generator is connected to a corresponding digital-to-
10 analog converter by the delay module, and the arbitrary waveform generator is further configured to synchronously send valid data to the corresponding digital-to-analog converter according to an associated clock sent by the corresponding digital-to-analog converter.

10. The signal generating apparatus of any one of claims 1 to 8, further comprising a service
15 decoding module, wherein the service decoding module is connected to a host, the external clock chip, the read-write control module, and the arbitrary waveform generator, respectively, and the service decoding module is configured to perform parameter configuration on the external clock chip and the arbitrary waveform generator according to an instruction sent from the host, and store the original waveform into the storage apparatus by the read-write control
20 module.

11. A signal generating method, characterized by comprising:

an external clock chip outputting a sampling clock to a digital-to-analog converter,
wherein the sampling clock has a fixed frequency;

5 a read-write control module reading an original waveform from a storage apparatus
according to a received read request instruction, and returning the read original waveform to
an arbitrary waveform generator; and

the arbitrary waveform generator performing resampling on the received original
waveform to generate a reconstructed waveform that is fitted with the frequency of the
10 sampling clock, wherein the reconstructed waveform is configured to perform digital-to-
analog conversion by the digital-to-analog converter according to the sampling clock output
from the external clock chip.

12. An analog-to-digital mixed test board, characterized by comprising the signal generating
15 apparatus of any one of claims 1 to 10.

13. A tester, characterized by comprising a communicating board, a back board, and the
analog-to-digital mixed test board of claim 12.