ABSTRACT OF THE DISCLOSURE

A dual damascene process is provided. A dielectric layer is formed on a substrate and then a via opening is formed in the dielectric layer to expose a liner formed on the substrate. A gap fill (GF) layer is filled into the via opening and a resistant layer is formed on the substrate. A photolithographic process and an etching process are performed to form a trench in the dielectric layer and to remain the gap fill material having a top surface with a convex shape. In the etching process, an etching rate of the gap fill material layer is larger than that of the resistant layer. The gap fill material, the resistant layer, and the liner exposed by the via opening are removed. A conductive layer fills out the trench and the via opening. This invention is focusing on controlling etch-rate to avoid shielding effect when forming the composite opening.

Figure 3A