

from the main body portion. The first bonding pads are connected to the main body portion and the extension portion. The number of the first bonding pads connected to the terminal portion of the extension portion is plural.

[0005] According to an embodiment of the invention, in the semiconductor structure, the number of the first bonding pads connected to the extension portion may be less than the number of the first bonding pads connected to the main body portion.

[0006] According to an embodiment of the invention, in the semiconductor structure, the number of the first bonding pads connected to the terminal portion of the extension portion may be less than the number of the first bonding pads connected to the main body portion.

[0007] According to an embodiment of the invention, in the semiconductor structure, the width of the terminal portion of the extension portion may be greater than the width of the rest of the extension portion.

[0008] According to an embodiment of the invention, in the semiconductor structure, the first bonding pads connected to the terminal portion of the extension portion may be arranged in a single direction.

[0009] According to an embodiment of the invention, in the semiconductor structure, the first bonding pads connected to the terminal portion of the extension portion may be arranged in an array.

[0010] According to an embodiment of the invention, the semiconductor structure may further include a first dielectric layer. The first dielectric layer is located on the first substrate. The first conductive layer and the first bonding pads may be located in the first dielectric layer.

[0011] According to an embodiment of the invention, the semiconductor structure may further include at least one second conductive layer and second bonding pads. The second conductive layer is located on the first substrate. The second bonding pads are connected to the second conductive layer.

[0012] According to an embodiment of the invention, in the semiconductor structure, the second

conductive layer may be adjacent to the terminal portion of the extension portion.

[0013] According to an embodiment of the invention, in the semiconductor structure, the second conductive layer and the second bonding pads may be located in the first dielectric layer.

5 **[0014]** According to an embodiment of the invention, the semiconductor structure may further include a second substrate, a third conductive layer, and third bonding pads. The first substrate may be located on the second substrate. The third conductive layer is located on the second substrate. The third bonding pads are connected to the third conductive layer.

[0015] According to an embodiment of the invention, in the semiconductor structure, a portion of the first bonding pads may be bonded to the third bonding pads.

10 **[0016]** According to an embodiment of the invention, the semiconductor structure may further include a second dielectric layer. The second dielectric layer is located on the second substrate. The third conductive layer and the third bonding pads may be located in the second dielectric layer.

[0017] According to an embodiment of the invention, in the semiconductor structure, the first dielectric layer may be bonded to the second dielectric layer.

15 **[0018]** According to an embodiment of the invention, the semiconductor structure may further include at least one fourth conductive layer and fourth bonding pads. The fourth conductive layer is located on the second substrate. The fourth bonding pads are connected to the fourth conductive layer.

20 **[0019]** According to an embodiment of the invention, in the semiconductor structure, the fourth conductive layer and the fourth bonding pads may be located in the second dielectric layer.

[0020] According to an embodiment of the invention, in the semiconductor structure, a portion of the first bonding pads may be bonded to a portion of the fourth bonding pads. The second bonding pads may be bonded to another portion of the fourth bonding pads.

25 **[0021]** According to an embodiment of the invention, in the semiconductor structure, a portion of the vertical projection of the first conductive layer may fall on the third conductive layer. Another portion of the vertical projection of the first conductive layer may fall on the fourth

conductive layer. A portion of the vertical projection of the second conductive layer may fall on the fourth conductive layer.

[0022] According to an embodiment of the invention, the semiconductor structure may further include at least one fifth conductive layer and at least one fifth bonding pad. The fifth conductive layer is located on the second substrate. The fifth bonding pad is connected to the fifth conductive layer.

[0023] According to an embodiment of the invention, in the semiconductor structure, a portion of the first bonding pads may be bonded to the fifth bonding pad.

[0024] Based on the above description, the semiconductor structure according to the invention includes the first conductive layer and the first bonding pads. The first conductive layer includes the main body portion and the extension portion. The extension portion is connected to the main body portion and includes the terminal portion away from the main body portion. Since the number of the first bonding pads connected to the terminal portion of the extension portion is plural, the galvanic corrosion occurring on the first bonding pad connected to the terminal portion of the extension portion can be effectively mitigated, thereby preventing the first bonding pad connected to the terminal portion of the extension portion from bonding failure in the subsequent bonding process.

[0025] In order to make the aforementioned and other objects, features and advantages of the invention comprehensible, several exemplary embodiments accompanied with drawings are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0027] FIG. 1 is a cross-sectional view illustrating a semiconductor structure according to some embodiments of the invention.

[0028] FIG. 2 is a top view illustrating the conductive layers and the bonding pads in FIG. 1.

[0029] FIG. 3 is a cross-sectional view illustrating a semiconductor structure according to other
5 embodiments of the invention.

[0030] FIG. 4 is a top view illustrating the conductive layers and the bonding pads in FIG. 3.

[0031] FIG. 5 is a cross-sectional view illustrating a semiconductor structure according to other
embodiments of the invention.

[0032] FIG. 6 is a top view illustrating the conductive layers and the bonding pads in FIG. 5.

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DESCRIPTION OF THE EMBODIMENTS

[0033] The embodiments are described in detail below with reference to the accompanying drawings, but the embodiments are not intended to limit the scope of the invention. For the sake of easy understanding, the same components in the following description will be denoted by the
15 same reference symbols. In addition, the drawings are for illustrative purposes only and are not drawn to the original dimensions. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0034] FIG. 1 is a cross-sectional view illustrating a semiconductor structure according to some
embodiments of the invention. FIG. 2 is a top view illustrating the conductive layers and the
20 bonding pads in FIG. 1. FIG. 1 is a cross-sectional view taken along section line I-I' in FIG. 2.

[0035] Referring to FIG. 1 and FIG. 2, the semiconductor structure 10 includes a substrate 100,
a conductive layer 102, and bonding pads 104. The substrate 100 may be a semiconductor
substrate such as a silicon substrate. In addition, although not shown in the figure, the substrate
100 may have required components thereon, such as semiconductor devices (e.g., active devices
25 and/or passive devices), and the description thereof is omitted here.

[0036] The conductive layer 102 is located on the substrate 100. The conductive layer 102

includes a main body portion P1 and an extension portion P2. The extension portion P2 is connected to the main body portion P1 and includes a terminal portion TP1 away from the main body portion P1. The extension portion P2 may extend in a direction D1 away from the main body portion P1. In addition, the top-view pattern of the conductive layer 102 is not limited to the pattern of FIG. 2. As long as the conductive layer 102 includes the main body portion P1 and the extension portion P2, it falls within the scope of the invention. The material of the conductive layer 102 is, for example, a conductive material such as copper.

[0037] The bonding pads 104 are connected to the main body portion P1 and the extension portion P2. The number of the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 is plural. Therefore, the galvanic corrosion occurring on the bonding pad 104 connected to the terminal portion TP1 of the extension portion P2 can be effectively mitigated, thereby preventing the bonding pad 104 connected to the terminal portion TP1 of the extension portion P2 from bonding failure in the subsequent bonding process. In some embodiments, the number of the bonding pads 104 connected to the extension portion P2 may be less than the number of the bonding pads 104 connected to the main body portion P1. In some embodiments, the number of the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 may be less than the number of the bonding pads 104 connected to the main body portion P1. In addition, the number of the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 is not limited to the number in the figure. As long as the number of the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 is plural, it falls within the scope of the invention. In some embodiments, the width W1 of the terminal portion TP1 of the extension portion P2 may be equal to the width W2 of the rest of the extension portion P2. In some embodiments, the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 may be arranged in a single direction (e.g., direction D1). The bonding pad 104 may be a single-layer structure or a multilayer structure. The material of the bonding pad 104 is, for example, copper, tantalum, tantalum nitride, or a combination thereof.

[0038] The semiconductor structure 10 may further include a dielectric layer 106. The dielectric layer 106 is located on the substrate 100. The conductive layer 102 and the bonding pads 104 may be located in the dielectric layer 106. In some embodiments, the dielectric layer 106 may be a multilayer structure. In addition, although not shown in the figure, the dielectric layer 106 may have required components therein, such as interconnect structures, and the description thereof is omitted here. The material of the dielectric layer 106 is, for example, silicon oxide, silicon nitride, silicon oxynitride, or a combination of related insulating materials.

[0039] The semiconductor structure 10 may further include at least one conductive layer 108 and bonding pads 110. The conductive layer 108 is located on the substrate 100. The conductive layer 108 may be located in the dielectric layer 106. The conductive layer 108 may be adjacent to the terminal portion TP1 of the extension portion P2. In the present embodiment, the number of the conductive layers 108 is, for example, plural, but the invention is not limited thereto. As long as the number of the conductive layers 108 is at least one, it falls within the scope of the invention. The material of the conductive layer 108 is, for example, a conductive material such as copper.

[0040] The bonding pads 110 are connected to the conductive layer 108. The bonding pads 110 may be located in the dielectric layer 106. In some embodiments, a plurality of the bonding pads 110 may be connected to the same conductive layer 108. The bonding pad 110 may be a single-layer structure or a multilayer structure. The material of the bonding pad 110 is, for example, copper, tantalum, tantalum nitride, or a combination thereof.

[0041] The semiconductor structure 10 may further include a substrate 200, a conductive layer 202, and bonding pads 204. The substrate 100 may be located on the substrate 200. The substrate 200 may be a semiconductor substrate such as a silicon substrate. In addition, although not shown in the figure, the substrate 200 may have required components thereon, such as semiconductor devices (e.g., active devices and/or passive devices), and the description thereof is omitted here.

[0042] The conductive layer 202 is located on the substrate 200. In some embodiments, a portion of the vertical projection of the conductive layer 102 may fall on the conductive layer 202. The material of the conductive layer 202 is, for example, a conductive material such as copper.

[0043] The bonding pads 204 are connected to the conductive layer 202. A portion of the bonding pads 104 may be bonded to the bonding pads 204. The bonding pad 204 may be a single-layer structure or a multilayer structure. The material of the bonding pad 204 is, for example, copper, tantalum, tantalum nitride, or a combination thereof.

[0044] The semiconductor structure 10 may further include a dielectric layer 206. The dielectric layer 206 is located on the substrate 200. The dielectric layer 106 may be bonded to the dielectric layer 206. The conductive layer 202 and the bonding pads 204 may be located in the dielectric layer 206. In some embodiments, the dielectric layer 206 may be a multilayer structure. In addition, although not shown in the figure, the dielectric layer 206 may have required components therein, such as interconnect structures, and the description thereof is omitted here. The material of the dielectric layer 206 is, for example, silicon oxide, silicon nitride, silicon oxynitride, or a combination of related insulating materials.

[0045] The semiconductor structure 10 may further include at least one conductive layer 208 and bonding pads 210. The conductive layer 208 is located on the substrate 200. The conductive layer 208 may be located in the dielectric layer 206. Another portion of the vertical projection of the conductive layer 102 may fall on the conductive layer 208. A portion of the vertical projection of the conductive layer 108 may fall on the conductive layer 208. In the present embodiment, the number of the conductive layers 208 is, for example, plural, but the invention is not limited thereto. As long as the number of the conductive layers 208 is at least one, it falls within the scope of the invention. The material of the conductive layer 208 is, for example, a conductive material such as copper.

[0046] The bonding pads 210 are connected to the conductive layer 208. The bonding pads 210 may be located in the dielectric layer 206. In some embodiments, a plurality of the bonding

pads 210 may be connected to the same conductive layer 208. A portion of the bonding pads 104 may be bonded to a portion of the bonding pads 210. The bonding pads 110 may be bonded to another portion of the bonding pads 210. The bonding pad 210 may be a single-layer structure or a multilayer structure. The material of the bonding pad 210 is, for example, copper, tantalum, 5 tantalum nitride, or a combination thereof.

[0047] In some embodiments, the conductive layer 102, the conductive layer 202, the conductive layer 108, and the conductive layer 208 may be electrically connected to each other by the bonding pad 104, the bonding pad 204, the bonding pad 110, and the bonding pad 210.

[0048] Based on the above embodiments, the semiconductor structure 10 includes the 10 conductive layer 102 and the bonding pads 104. The conductive layer 102 includes the main body portion P1 and the extension portion P2. The extension portion P2 is connected to the main body portion P1 and includes the terminal portion TP1 away from the main body portion P1. Since the number of the bonding pads 104 connected to the terminal portion TP1 of the extension portion P2 is plural, the galvanic corrosion occurring on the bonding pad 104 connected to the 15 terminal portion TP1 of the extension portion P2 can be effectively mitigated, thereby preventing the bonding pad 104 connected to the terminal portion TP1 of the extension portion P2 from bonding failure in the subsequent bonding process.

[0049] FIG. 3 is a cross-sectional view illustrating a semiconductor structure according to other embodiments of the invention. FIG. 4 is a top view illustrating the conductive layers and the 20 bonding pads in FIG. 3. FIG. 3 is a cross-sectional view taken along section line II-II' in FIG. 4.

[0050] Referring to FIG. 1 to FIG. 4, the difference between a semiconductor structure 20 and the semiconductor structure 10 is as follows. In the semiconductor structure 20, the width W3 of the terminal portion TP2 of the extension portion P2 may be greater than the width W2 of the rest of the extension portion P2. In some embodiments, the terminal portion TP2 of the extension 25 portion P2 may extend in a direction D2 and a direction D3, that is, the extension direction of the extension portion P2 is turned at the terminal portion TP2. In some embodiments, the direction

D2 and the direction D3 may intersect the direction D1. In the semiconductor structure 20, the bonding pads 104 connected to the terminal portion TP2 of the extension portion P2 may be arranged in an array. In addition, the number of the bonding pads 104 connected to the terminal portion TP2 of the extension portion P2 is not limited to the number in the figure. As long as the number of the bonding pads 104 connected to the terminal portion TP2 of the extension portion P2 is plural, it falls within the scope of the invention. In some embodiments, a portion of the conductive layer 208 corresponding to the terminal portion TP2 may have a width W4, a portion of the conductive layer 208 corresponding to the conductive layer 108 may have a width W5, and the width W4 may be greater than the width W5.

[0051] In addition, in the semiconductor structure 10 and the semiconductor structure 20, the same or similar components are denoted by the same reference symbols, and the description thereof is omitted.

[0052] Based on the above embodiments, the semiconductor structure 20 includes the conductive layer 102 and the bonding pads 104. The conductive layer 102 includes the main body portion P1 and the extension portion P2. The extension portion P2 is connected to the main body portion P1 and includes the terminal portion TP2 away from the main body portion P1. Since the number of the bonding pads 104 connected to the terminal portion TP2 of the extension portion P2 is plural, the galvanic corrosion occurring on the bonding pad 104 connected to the terminal portion TP2 of the extension portion P2 can be effectively mitigated, thereby preventing the bonding pad 104 connected to the terminal portion TP2 of the extension portion P2 from bonding failure in the subsequent bonding process.

[0053] FIG. 5 is a cross-sectional view illustrating a semiconductor structure according to other embodiments of the invention. FIG. 6 is a top view illustrating the conductive layers and the bonding pads in FIG. 5. FIG. 5 is a cross-sectional view taken along section line III-III' and section line IV-IV' in FIG. 6.

[0054] Referring to FIG. 1, FIG. 2, FIG. 5, and FIG. 6, the difference between the semiconductor

structure 30 and the semiconductor structure 10 is as follows. In the semiconductor structure 30, the width W6 of the terminal portion TP3 of the extension portion P2 may be greater than the width W2 of the rest of the extension portion P2. In some embodiments, the terminal portion TP3 of the extension portion P2 may extend in a direction D4, that is, the extension direction of the extension portion P2 is turned at the terminal portion TP3. In some embodiments, the direction D4 may intersect the direction D1. In some embodiments, the bonding pads 104 connected to the terminal portion TP3 of the extension portion P2 may be arranged in a single direction (e.g., direction D4). In addition, the number of the bonding pads 104 connected to the terminal portion TP3 of the extension portion P2 is not limited to the number in the figure. As long as the number of the bonding pads 104 connected to the terminal portion TP3 of the extension portion P2 is plural, it falls within the scope of the invention.

[0055] In some embodiments, the semiconductor structure 30 may further include at least one conductive layer 212 and at least one bonding pad 214. The conductive layer 212 is located on the substrate 200. The conductive layer 212 may be located in the dielectric layer 206. Another portion of the vertical projection of the conductive layer 102 may fall on the conductive layer 212. In the present embodiment, the number of the conductive layers 212 is plural, but the invention is not limited thereto. As long as the number of the conductive layers 212 is at least one, it falls within the scope of the invention. The material of the conductive layer 212 is, for example, a conductive material such as copper.

[0056] The bonding pad 214 is connected to the conductive layer 212. The bonding pads 214 may be located in the dielectric layer 206. A portion of the bonding pads 104 may be bonded to the bonding pads 214. The bonding pad 214 may be a single-layer structure or a multilayer structure. In the present embodiment, the number of the bonding pads 214 is, for example, plural, but the invention is not limited thereto. As long as the number of the bonding pads 214 is at least one, it falls within the scope of the invention. The material of the bonding pad 214 is, for example, copper, tantalum, tantalum nitride, or a combination thereof.

[0057] In other embodiments, the semiconductor structure 30 may not include the conductive layer 212 and the bonding pads 214. In other embodiments, the semiconductor structure 30 may include the conductive layer 212, and the semiconductor structure 30 may not include the bonding pads 214.

5 **[0058]** In addition, in the semiconductor structure 10 and the semiconductor structure 30, the same or similar components are denoted by the same reference symbols, and the description thereof is omitted.

[0059] Based on the above embodiments, the semiconductor structure 30 includes the conductive layer 102 and the bonding pads 104. The conductive layer 102 includes the main
10 body portion P1 and the extension portion P2. The extension portion P2 is connected to the main body portion P1 and includes the terminal portion TP3 away from the main body portion P1. Since the number of the bonding pads 104 connected to the terminal portion TP3 of the extension portion P2 is plural, the galvanic corrosion occurring on the bonding pad 104 connected to the terminal portion TP3 of the extension portion P2 can be effectively mitigated, thereby preventing
15 the bonding pad 104 connected to the terminal portion TP3 of the extension portion P2 from bonding failure in the subsequent bonding process.

[0060] In summary, the semiconductor structure in the above embodiment includes the conductive layer and the bonding pads. The conductive layer includes the main body portion and the extension portion. The extension portion is connected to the main body portion and
20 includes the terminal portion away from the main body portion. Since the number of the bonding pads connected to the terminal portion of the extension portion is plural, the galvanic corrosion occurring on the bonding pad connected to the terminal portion of the extension portion can be effectively mitigated, thereby preventing the bonding pad connected to the terminal portion of the extension portion from bonding failure in the subsequent bonding process.

25 **[0061]** Although the invention has been described with reference to the above embodiments, it will be apparent to one of ordinary skill in the art that modifications to the described embodiments

may be made without departing from the spirit of the invention. Accordingly, the scope of the invention is defined by the attached claims not by the above detailed descriptions.

CLAIMS

WHAT IS CLAIMED IS:

[CLAIM 1]

A semiconductor structure, comprising:

5 a first substrate;

a first conductive layer located on the first substrate and comprising:

a main body portion; and

an extension portion connected to the main body portion and comprising a terminal portion away from the main body portion; and

10 first bonding pads connected to the main body portion and the extension portion, wherein the number of the first bonding pads connected to the terminal portion of the extension portion is plural.

[CLAIM 2]

15 The semiconductor structure according to claim 1, wherein the number of the first bonding pads connected to the extension portion is less than the number of the first bonding pads connected to the main body portion.

[CLAIM 3]

20 The semiconductor structure according to claim 1, wherein the number of the first bonding pads connected to the terminal portion of the extension portion is less than the number of the first bonding pads connected to the main body portion.

[CLAIM 4]

25 The semiconductor structure according to claim 1, wherein a width of the terminal portion of the extension portion is greater than a width of the rest of the extension portion.

[CLAIM 5]

The semiconductor structure according to claim 1, wherein the first bonding pads connected to the terminal portion of the extension portion are arranged in a single direction.

5 [CLAIM 6]

The semiconductor structure according to claim 1, wherein the first bonding pads connected to the terminal portion of the extension portion are arranged in an array.

[CLAIM 7]

10 The semiconductor structure according to claim 1, further comprising:
a first dielectric layer located on the first substrate, wherein the first conductive layer and the first bonding pads are located in the first dielectric layer.

[CLAIM 8]

15 The semiconductor structure according to claim 7, further comprising:
at least one second conductive layer located on the first substrate; and
second bonding pads connected to the second conductive layer.

[CLAIM 9]

20 The semiconductor structure according to claim 8, wherein the second conductive layer is adjacent to the terminal portion of the extension portion.

[CLAIM 10]

25 The semiconductor structure according to claim 8, wherein the second conductive layer and the second bonding pads are located in the first dielectric layer.

[CLAIM 11]

The semiconductor structure according to claim 8, further comprising:

a second substrate, wherein the first substrate is located on the second substrate;

a third conductive layer located on the second substrate; and

5 third bonding pads connected to the third conductive layer.

[CLAIM 12]

The semiconductor structure according to claim 11, wherein a portion of the first bonding pads is bonded to the third bonding pads.

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[CLAIM 13]

The semiconductor structure according to claim 11, further comprising:

a second dielectric layer located on the second substrate, wherein the third conductive layer and the third bonding pads are located in the second dielectric layer.

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[CLAIM 14]

The semiconductor structure according to claim 13, wherein the first dielectric layer is bonded to the second dielectric layer.

20 [CLAIM 15]

The semiconductor structure according to claim 13, further comprising:

at least one fourth conductive layer located on the second substrate; and

fourth bonding pads connected to the fourth conductive layer.

25 [CLAIM 16]

The semiconductor structure according to claim 15, wherein the fourth conductive layer and

the fourth bonding pads are located in the second dielectric layer.

[CLAIM 17]

The semiconductor structure according to claim 15, wherein

5 a portion of the first bonding pads is bonded to a portion of the fourth bonding pads, and
the second bonding pads are bonded to another portion of the fourth bonding pads.

[CLAIM 18]

The semiconductor structure according to claim 15, wherein

10 a portion of a vertical projection of the first conductive layer falls on the third conductive
layer,

another portion of the vertical projection of the first conductive layer falls on the fourth
conductive layer, and

a portion of a vertical projection of the second conductive layer falls on the fourth
15 conductive layer.

[CLAIM 19]

The semiconductor structure according to claim 15, further comprising:

at least one fifth conductive layer located on the second substrate; and

20 at least one fifth bonding pad, wherein the fifth bonding pad is connected to the fifth
conductive layer.

[CLAIM 20]

The semiconductor structure according to claim 19, wherein a portion of the first bonding

25 pads is bonded to the fifth bonding pad.