CLAIMS

1. A thermalization structure, comprising:

a cover configured with a set of pillars, the cover being a part of a cryogenic enclosure of a low temperature device (LTD) operating in a cryogenic temperature range;

a chip comprising the LTD, the chip configured with a set of cavities, a cavity in the set of cavities having a cavity profile, wherein a pillar from the set of pillars and corresponding to the cavity has a pillar profile such that the pillar profile causes the pillar to couple with the cavity of the cavity profile within a gap tolerance to thermally couple the chip to the cover for heat dissipation in a cryogenic operation of the chip.

2. The thermalization structure of claim 1, wherein a subset of the set of pillars is coupled with a subset of the set of cavities to form a~~the~~ thermal coupling between the chip and the cover.

3. The thermalization structure of claim 1, wherein a first pillar in the set of pillars has a different cross-section than a second pillar in the set of pillars.

4. The thermalization structure of claim 1, wherein a first pillar in the set of pillars has a different height than a second pillar in the set of pillars.

5. The thermalization structure of claim 1, wherein a first subset of pillars in the set of pillars has a different pillar density per unit of area of a designated surface of the cover than a second subset of pillars in the set of pillars on the designated surface.

6. The thermalization structure of claim 1, wherein the chip comprises a flip-chip assembly, the thermalization structure further comprising:

a second cover configured with a second set of pillars, the second cover being a part of the cryogenic enclosure; and

a second chip in the flip-chip configuration, the second chip configured with a second set of cavities, a second cavity in the second set of cavities having a second cavity profile, wherein a second pillar from the second set of pillars and corresponding to the second cavity has a second pillar profile such that the second pillar profile causes the second pillar to couple with the second cavity of the second cavity profile within a second gap tolerance to thermally couple the second chip to the second cover for heat dissipation in a cryogenic operation of the flip-chip.

7. The thermalization structure of claim 1, wherein a first pillar in the set of pillars is configured to align the chip with a designated surface on the cover, and a second pillar in the set of pillars is configured to operate as a thermal conductor.

8. The thermalization structure of claim 1, wherein a cross-sectional shape of the cavity is determined by a location of the cavity on a thermal surface of the chip.

9. The thermalization structure of claim 1, wherein a cross-sectional area of the cavity is determined by a location of the LTD on the chip.

10. The thermalization structure of claim 1, wherein a depth of the cavity is determined by a location of the LTD on the chip.

11. The thermalization structure of claim 1, wherein a first cavity in the set of cavities has a different cross-section than a second cavity in the set of cavities.

12. The thermalization structure of claim 1, wherein a first cavity in the set of cavities has a different depth than a second cavity in the set of cavities.

13. The thermalization structure of claim 1, wherein a first subset of cavities in the set of cavities has a different cavity density per unit of area of a thermal surface of the chip than a second subset of cavities in the set of cavities on the thermal surface.

14. The thermalization structure of claim 1, wherein a first cavity in the set of cavities is configured to align the chip with a designated surface on the cover, and a second cavity in the set of cavities is configured to thermalize the chip with the cover.

15. The thermalization structure of claim 1, further comprising:

a liner in a cavity from the set of cavities, wherein the liner comprises a material that is a better thermal conductor than a substrate material of the chip in thea cryogenic temperature range.

16. The thermalization structure of claim 15, wherein the liner is deposited on a first surface of the cavity but not on a second surface of the cavity.

17. The thermalization structure of claim 1, further comprising:

a liner on a pillar from the set of pillars, wherein the liner comprises a material that is a better thermal conductor than a substrate material of the cover in thea cryogenic temperature range.

18. The thermalization structure of claim 17, wherein the liner is deposited on a first surface of the pillar but not on a second surface of the pillar.

19. A computer-implemented method for fabricating a thermalization structure, the computer-implemented method comprising:

forming a cover configured with a set of pillars, the cover being a part of a cryogenic enclosure of a low temperature device (LTD) operating in a cryogenic temperature range;

forming set of cavities in a chip comprising the LTD, a cavity in the set of cavities having a cavity profile, wherein a pillar from the set of pillars and corresponding to the cavity has a pillar profile; and

forming, responsive to the pillar with the pillar profile coupling with the cavity of the cavity profile within a gap tolerance, a thermal coupling between the chip and the cover for heat dissipation in a cryogenic operation of the chip.

20. The computer-implemented method of claim 19, wherein a subset of the set of pillars is coupled with a subset of the set of cavities to form the thermal coupling between the chip and the cover.

21. The computer-implemented method of claim 19, wherein a first pillar in the set of pillars has a different cross-section than a second pillar in the set of pillars.

22. The computer-implemented method of claim 19, wherein a first pillar in the set of pillars has a different height than a second pillar in the set of pillars.

23. A semiconductor fabrication system for fabricating a thermalization structure, the semiconductor fabrication system comprising

a component which when operated by a processor causes a fabrication method to be performed, the fabrication method comprising:

forming a cover configured with a set of pillars, the cover being a part of a cryogenic enclosure of a low temperature device (LTD) operating in a cryogenic temperature range;

forming set of cavities in a chip comprising the LTD, a cavity in the set of cavities having a cavity profile, wherein a pillar from the set of pillars and corresponding to the cavity has a pillar profile; and

forming, responsive to the pillar with the pillar profile coupling with the cavity of the cavity profile within a gap tolerance, a thermal coupling between the chip and the cover for heat dissipation in a cryogenic operation of the chip.

24. A quantum processor, comprising:

a thermalization structure, the thermalization structure comprising:

a cover configured with a set of pillars, the cover being a part of a cryogenic enclosure of a qubit chip;

the qubit chip comprising a qubit, the qubit chip configured with a set of cavities, a cavity in the set of cavities having a cavity profile, wherein a pillar from the set of pillars and corresponding to the cavity has a pillar

profile such that the pillar profile causes the pillar to couple with the cavity of the cavity profile within a gap tolerance to thermally couple the chip to the cover for heat dissipation in a cryogenic operation of the chip.

25. A quantum data processing system, comprising:

a quantum processor;

a thermalization structure coupled with the quantum processor, comprising:

a cover configured with a set of pillars, the cover being a part of a cryogenic enclosure of a qubit chip;

the qubit chip comprising a qubit, the qubit chip configured with a set of cavities, a cavity in the set of cavities having a cavity profile, wherein a pillar from the set of pillars and corresponding to the cavity has a pillar profile such that the pillar profile causes the pillar to couple with the cavity of the cavity profile within a gap tolerance to thermally couple the qubit chip to the cover for heat dissipation in a cryogenic operation of the qubit chip.