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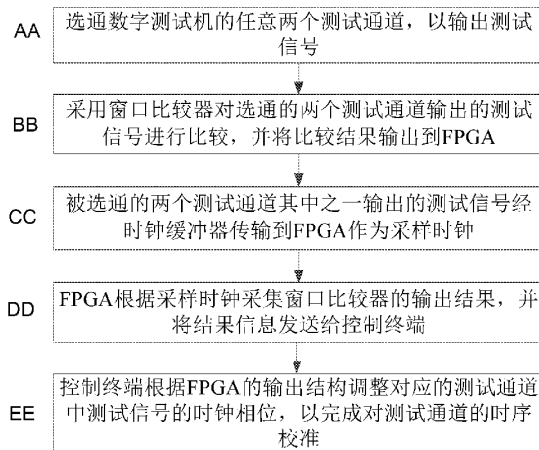
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(54) Title: TIMING CALIBRATION METHOD AND SYSTEM

(54) 发明名称: 一种时序校准方法和系统



AA Gate any two test channels of a digital test machine, so as to output test signals
BB Compare, by using a window comparator, the test signals output by the two gated test channels, and output a comparison result to an FPGA
CC Transmit, to the FPGA and via a clock buffer, the test signal output by one of the two gated test channels, and take the test signal as a sampling clock
DD The FPGA collects the output result of the window comparator according to the sampling clock, and sends result information to a control terminal
EE The control terminal adjusts a clock phase of the test signal in the corresponding test channel according to an output structure of the FPGA, so as to complete timing calibration of the test channel

图 2

(57) Abstract: Disclosed in the present invention are a timing calibration method and system. The timing calibration method is used for performing timing calibration on test signals in a plurality of test channels of a digital test machine. The method comprises: gating any two test channels of a digital test machine, so as to output test signals; comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to an FPGA; transmitting, to the FPGA and via a clock buffer, the test signal output by one of the two gated test channels, and taking the test signal as a sampling clock; the FPGA collecting the output result of the window comparator according to the sampling clock, and sending result information to a control terminal; and the control terminal adjusting a clock phase of the test signal in the corresponding test channel according to an output structure of the FPGA, so as to complete timing calibration of the test channel.

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TD, TG)。

本国际公布:

— 包括国际检索报告 (条约第21条(3))。

(57) 摘要: 本发明公开一种时序校准方法和系统, 该时序校准方法, 用于对数字测试机的若干测试通道中的测试信号进行时序校准, 该方法包括: 选通数字测试机的任意两个测试通道, 以输出测试信号; 采用窗口比较器对选通的两个测试通道输出的测试信号进行比较, 并将比较结果输出到FPGA; 被选通的两个测试通道其中之一输出的测试信号经时钟缓冲器传输到FPGA作为采样时钟; FPGA根据采样时钟采集窗口比较器的输出结果, 并将结果信息发送给控制终端; 控制终端根据FPGA的输出结构调整对应的测试通道中测试信号的时钟相位, 以完成对测试通道的时序校准。