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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES WITH STEPPING MOTOR DRIVEN ANALOG TIME DISPLAYS

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention, which is for improvements in or modifications of the invention contained in the parent specification No. 47462/77, (Serial No. 1592892), relates to electronic timepieces having stepping motor driven analog time displays.

According to the parent invention a stepping motor electronic timepiece comprises in combination a time standard oscillator; a frequency divider for dividing in frequency time standard oscillations from said oscillator; a pulse combining circuit for producing normal drive pulses of a pre-determined width for normally driving the motor and correction drive pulses of increased width relative to that of said normal drive pulses; a detecting circuit, operating after a normal drive pulse has been applied to said motor for detecting whether the condition of rotation, or non-rotation is present in the motor; and means, controlled by said detection circuit, for supplying a correction drive pulse to said motor to force it to rotate correctly before the application thereto of the next normal drive pulse.

The parent specification describes and illustrates arrangements in which the motor is of the type having a driving coil magnetically linked with a stator formed as a single integral body providing a saturable magnetic circuit and having a portion surrounding a permanently magnetised rotor with at least one pair of magnetic poles, the rest positions being positions in which a rotor diameter through opposite poles of a pair or of each pair of rotor poles is angularly displaced with respect to a line in which lie opposite poles produced in the stator when a driving pulse is applied to the coil thereof. The driving pulses applied to the motor are all of the same amplitude, increase in driving pulse power produced when the condition of non-rotation is detected being obtained by increasing the pulse length.

The present invention is illustrated in and explained in connection with the accompanying drawings in which:—

Figure 1 shows part of the time display driving mechanism of a typical known electronic watch with a stepping motor, which is as illustrated in the parent specification driving an analog time display;

Figure 2 is a block diagram of a conventional known watch having a display driving mechanism as represented in Figure 1;

Figures 3, 7, 8, 14, 17 and 18 are explanatory graphical figures;

Figures 4, 5 and 6 are figures which are used to aid explanation of certain actions which take place in the stepping motor when in operation;

Figure 9 is a block diagram of one embodiment of the invention;

Figure 10 is a block diagram representation of the circuit 53 of Figure 9;

Figure 12 shows some of the circuitry employed in the block diagram of Figure 9;

Figures 11 and 13 show waveforms occurring in Figures 9 and 12;

Figure 15 shows the circuitry of the comparator 110 of Figure 12; and

Figure 16 is a block diagram showing the comparator 110 separately.

Figure 1 shows part of the analog time display driving mechanism of a typical known electronic watch in which the time display is driven by the stepping electric

motor illustrated in that Figure. The said motor comprises a stator 1, with a driving coil 7 on a limb thereof and a permanently magnetised rotor 6 having magnetic poles N, S. The rotor drives through gears 2, 3, 4, 5 (and, if required, further gears not shown) a wheel on which the seconds hand is fixed. The seconds hand wheel drives, through further gearing, a minutes hand, an hours hand and a calendar. The hands and the calendar are not shown in Figure 1, nor is the gearing beyond the wheel 2, but all this is well known and needs no illustration or description here.

In the case of a wrist watch with hands and a calendar, the load imposed on the stepping motor is extremely small except during the time in which the calendar is being changed. In practice this load is so small that a motor torque of only about 1.0 g/cm is sufficient to overcome it in a reliable manner. However, when the calendar is being changed the load on the motor is such as to require it to develop a torque which is two or more times that needed when the calendar is not being changed. The time taken to change the calendar is several hours but is at most only about 6 hours out of the 24. Normal practice is for the motor to be arranged to deliver, throughout the 24 hours, sufficient torque to overcome the maximum load on it—i.e. the load imposed when the calendar is being changed—despite that this load is actually imposed for, at most, only 6 hours out of the 24. This practice involves an undesirably high overall power consumption a considerable proportion of which is wasted. This is a serious defect, involving, as it does, a correspondingly shortened useful life of the battery which constitutes the power source of the watch. The parent invention overcomes this defect.

Figure 2 is a block diagram of a typical known analog type quartz crystal controlled electronic watch. Referring to Figure 2, block 10 is a quartz crystal controlled time standard oscillator of, for example, 32.768 KHz the output of which is fed to a frequency divider 11 consisting of a cascade series of flip-flops and producing a 1 Hz output. This output is passed to a pulse combining and forming circuit 12 which produces therefrom, on its respective output leads 15, 16, two pulsed wave forms which are dephased with respect to one another by one second and each of which has a pulse period of 2 seconds, with pulses of, for example, 7.8 m sec wide. These wave forms are passed through respective inverters 13*a*, 13*b* and applied to opposite ends of the motor coil 7. The arrangement is such that successively oppositely directed pulses of current are applied to the coil 7 every second, causing the two-pole permanently magnetized rotor 6 to rotate, always in the same direction, in a series of 1-second steps. Figure 3 shows the current wave form (I/T) through the coil during one applied current pulse. The width (typically 7.8 m sec) of the pulse is chosen at a value required to cause the motor always to develop the maximum torque required at any time during the 24 hours. Because this maximum torque is, however, actually required for, at most, 6 hours out of the 24, there is a substantial waste of overall electric power. As already stated the parent invention overcomes this defect.

Before defining and describing the present invention the principle of operation of the stepping motor illustrated in Fig. 1 and certain actions which occur therein when it is in operation will first be explained with the aid of Figures 4, 5, 6 and 7.

Figure 4 again shows the motor included in Figure 1. It has a stator 1 which is constructed as an integral body with a limb on which is the coil 7. The magnetic circuit of the stator includes portions 17*a*, 17*b* of restricted cross section which make the magnetic circuit easily magnetically saturable. The stator is provided with diametrically opposite notches 18*a*, 18*b* the angular positions of which determined the direction of the rotation of the rotor 6. In Figure 4 the rotor is shown in the position in which a current pulse is just being applied to the coil 7. When no current pulse is applied the rotor assumes a rest position in which the diameter in which the rotor poles N, S lie is approximately at right angles to the diameter joining the notches 18*a*, 18*b*. If, now, a current pulse is passed through the coil 7 in the direction indicated by the arrow heads thereon magnetic poles are produced in the stator 1 as indicated by the letters N, S on the stator and the rotor 6 rotates clockwise (as seen in Figure 4) by mutual repulsion between like poles. When the current pulse ceases, the rotor stops in a position opposite to that shown in Figure 4. If, now, a further pulse is passed through the coil 7 in a direction opposite to that indicated in Figure 4, the rotor will take another step in the same direction as before. Because, due to the presence of the restrictions 17*a*, 17*b* in the integral stator body, the stator is easily magnetically saturable, the current/time (I/T) wave form through the coil 7 presents a characteristic with an initial slowly rising curve as shown in Figure 3. The reason for this is that, before saturation occurs the magnetic resistance of the stator magnetic circuit, as seen from the coil 7, is very

small so that the time constant τ of a circuit including the coil and any resistance in series therewith (this, of course, necessarily includes the DC resistance of the coil itself) is very large. The time constant can be expressed by the equation:—

$$\tau = L/R;\ L \doteqdot N^2/R_m$$

where L is the coil inductance; R is the DC resistance in circuit; N is the number of turns in the coil; and R_m is the magnetic resistance of the magnetic circuit.

We may therefore write:—

$$\tau \doteqdot N^2/(R \times R_m)$$

When, however, the saturable portions 17*a*, 17*b* become saturated, the permeability becomes the same as that of air. Accordingly, R_m increases, the time constant τ of the circuit becomes small, and the current wave characteristic rises abruptly as shown in Figure 3.

Figure 5 shows magnetic fields set up when the rotor is in the position shown in Figure 4 and a current pulse in the direction indicated is applied to the coil. The rotor flux due to the permanently magnetised rotor 6 is represented by the flux lines 20*a*, 20*b*. There is also a magnetic flux which links with the coil 7 but this is not shown. The fluxes 20*a*, 20*b* pass through the saturable portions 17*a* and 17*b* in the directions indicated by the arrow heads on the flux lines. In most cases the portions 17*a*, 17*b* are, initially, well below saturation. When, however, current is passed through the coil in the direction indicated magnetic fluxes as indicated by the flux lines 19*a*, 19*b* are produced by the coil 7 and, as will be seen, these reinforce the rotor fluxes 20*a* and 20*b* in the saturable portions 17*a* and 17*b*, and these portions rapidly saturate. After this, magnetic flux sufficient for rotating the rotor 6 is produced but this is not shown. Figure 7 shows by curve 22 the wave form of the current through the coil. If the rotor is able to be rotated properly by the applied pulse (this condition is what is called herein the condition of rotation) the pulse causes the rotor to rotate through one step clockwise. Suppose, however, that for some reason—e.g. the load on the motor is too high to be overcome by the pulse applied—the rotor does not rotate properly but assumes, at the end of the pulse, the position it occupied when the pulse was applied. This is the condition of non-rotation. When the next pulse is applied the situation will be as represented in Figure 6, for the said next pulse is in the opposite direction to that in Figure 5, the direction of current flow through the coil 7 being now as indicated in Figure 6. The rotor flux directions through the saturable portions 17*a*, 17*b* are still as shown in Figure 5, but the stator poles N, S are reversed and the stator fluxes are as indicated by the flux lines 21*a* and 21*b* in Figure 6. As will be seen the rotor and stator fluxes now oppose one another in the saturable portions 17*a*, 17*b* and accordingly it takes a much longer time to achieve saturation. The current/time characteristic of current flow through the coil is accordingly very different from that shown by curve 22 of Figure 7 and is as shown by curve 23 of that figure. In a particular case of a motor with a coil 7 of 10000 turns and a diameter of 0.23 cms; a stator with restrictions of minimum width 0.1 cms; a rotor of 1.3 cms diameter, and a DC resistance of 3 KΩ in the coil circuit, the time D taken to achieve saturation was 1 m sec. As will now be appreciated from the curves 22 and 23 of Figure 7, the effective inductances presented by the coil 7 in the conditions of rotation and non-rotation are very different over the range C of Figure 7, being much larger in the latter condition than in the former. With the motor having the particular specification set out above the effective inductance L in the range D was 5 Henries in the condition of rotation (curve 22) but 40 Henries in the condition of non-rotation (curve 23). Such a large difference in effective inductance is easily detectable.

The present invention is concerned with the means for detecting the aforesaid difference in the effective inductance presented by the motor coil and according to the present invention an electronic timepiece as claimed in claim 1 of the parent specification includes in a detection circuit for detecting whether the motor is in the condition of rotation or of non-rotation a resistive detecting element in circuit with the drive coil of the motor so that the voltage drop across it is dependent on the effective inductance presented by said coil there being provided a comparator for comparing said voltage drop with a reference voltage.

Figure 9 is a block diagram of an electronic timepiece embodying the present invention. Referring to Figure 9, block 10 is a quartz crystal controlled time

standard oscillator of, for example, 32.768 KHz feeding its output into a frequency divider 11 consisting of a series of flip-flop stages and producing a 1 Hz output which is fed to a pulse combining and forming circuit 53. This circuit 53 receives and combines inputs taken from selected different stages of the frequency divider and produces therefrom what are herein termed normal drive pulses, i.e. pulses of a normal predetermined width sufficient to drive the stepping motor correctly when it operates against the normal load which is imposed on it for most of the 24 hours (some 18 hours or more) when the calendar is not being changed; what are herein termed correction drive pulses, i.e. pulses of greater predetermined width sufficient to drive the stepping motor correctly when it operates against the maximum load expected to be imposed on it (while the calendar is being changed); short detection pulses during which the condition of rotation or of non-rotation of the motor is detected; a time interval setting signal which determines the time interval between a normal drive pulse and a detection pulse, and a time interval setting signal which determines the time interval between a detection pulse and a correction drive pulse, 54 is a drive circuit which receives drive pulses from the pulse combining and forming circuit 53 and drives the stepping motor here represented by the block M. 56 is a detecting circuit which operates during a detection pulse to detect whether the condition of rotation or non-rotation exists in the motor and, in dependence upon which condition exists, applies a detected output signal to the pulse combining and forming circuit 53.

When the load on the motor is low, as it is for most of the time, the stepping motor is rotated by the less powerful (narrower) normal pulses. However, when the load on the motor becomes so high that the normal drive pulses are no longer sufficient to cause it to rotate correctly, and the condition of non-rotation is set up, This is detected by the detecting circuit 56 due to the increase in the effective inductance of the motor coil accompanying this condition and the detecting circuit accordingly applies to the pulse combining and forming circuit 53 a detected output signal which causes said circuit 53 to apply the wider correction drive pulses to the drive circuit 54. The motor thus develops the higher torque necessary to overcome the higher load thereon.

Figure 10 shows the circuit 53 as a separate block with input terminals Q_1 to Q_{15} and output terminals NP, DP and CP at which appear, respectively, 1-second normal drive pulses (as shown 3.9 m sec wide), short detection pulses $\emptyset$ of sufficient width (0.5 m sec wide) to enable detection of the motor condition (rotation or non-rotation) to be effected, and correction drive pulses (as shown 7.8 m sec wide). These outputs are obtained by arranging gates to combine wave forms obtained at different selected flip-flop stages in the divider 11. The combinations effected are set out below in a series of statements in which Q and $\overline{Q}$ refer to the Q and $\overline{Q}$ outputs of different flip-flop stages in the divider 11, the various states being identified by the numbers following the Q and $\overline{Q}$ references:—

for the 1 sec. normal drive pulses:— Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13} Q_{14}, and Q_{15}
for the 1 sec. correction drive pulses:— Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13}, Q_{14}, and Q_{15}
for the detection pulses $\emptyset$:— Q_5, Q_6, Q_7, Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13}, Q_{14}, and Q_{15}

If, as assumed, the frequency of the oscillator 10 is 32.768 KHz, the frequency at Q_5 is 1024 Hz, that at Q_4 is 512 Hz. . . and so on to Q_{15} where the frequency is 1 Hz. The wave form at Q_5, Q_6, Q_7, Q_8, Q_9, Q_{10}, Q_{11} and Q_{15} (with the relevant frequencies) are shown in the upper part of Figure 11, the lower part of which shows the combination wave forms at terminals NP, DP and CP.

Figure 12 shows the circuitry employed in the pulse combining and forming circuit 53, the drive circuit 54 and the detecting circuit 56 of Figure 9.

Block 100 is a flip-flop to the clock input terminal CL of which is applied the normal 1-second drive pulses from terminal NP. This flip-flop produces at its Q terminal a $\frac{1}{2}$ Hz output which is applied to one input of each of two NOR gates 102 and 103 and, at its $\overline{Q}$ terminal an opposite output which is applied to one input of each of two NOR gates 104 and 105. The 1-second pulses at terminal 130 are also applied to one input of a NOR gate 101. A 1-second correction drive pulses at terminal CP are applied through an inverter CP to the reset terminal R of an R-S flip-flop 112 which, if the condition of non-rotation exists, supplies them to the remaining input of NOR gate 101, the output of which is applied to the remaining inputs of the NOR gates 103 and 104.

Detection pulses $\emptyset$ appearing at terminal DP are applied through an inverter 120 to the remaining inputs of NOR gates 102 and 105, and also to the gate of an N

MOS FET 111 which, as will be seen later, is used for inhibiting a comparator.

The output of NOR gate 102 is applied to the gate of an N MOS FET 115 and also to one input of an OR gate 106.

The output of NOR gate 103 is applied to the gate of an N MOS FET 114 and also to the remaining input of OR gate 106.

The output of NOR gate 104 is applied to the gate of an N MOS FET 119 and also to one input of an OR gate 107.

The output of NOR gate 105 is applied to the gate of an N MOS FET 116 and also to one input of an OR gate 107.

The output of OR gate 106 is applied to the gate of a P MOS FET 113 while that of OR gate 107 is applied to the gate of a P MOS FET 118.

In Figure 12 the stepping motor is represented by its coil 7 which is connected at one end to the drains of the MOS FETs 113, 114 and 115 and at the other to the drains of the MOS FETs 116, 118 and 119.

The foregoing circuitry relates to the pulse combining and forming circuit 53. The circuitry of the drive circuit 54 and of the detection circuit 56 will now be described.

134 is the positive terminal of a power supply (battery) of voltage V_D and is connected to the sources of the MOS FETs 113 and 118. The negative terminal of the battery is grounded. The sources of MOS FETs 114 and 119 are grounded and connected to one end of a detecting resistor 117 the other end of which is connected to the common source connections of the MOS FETs 115, 116 and to the positive input terminal of a comparator 110. The drains of P MOS FETs 118, 119 are connected together and to one end of the motor coil 7 the other end of which is connected to the common source connection of N MOS FETs 115 and 116 and to the positive input terminal of comparator 110.

The positive input terminal 134 (shown twice in Figure 12) is connected to one end of a resistor 108 the other end of which is connected to one end of a resistor 109 and also to the negative input terminal of the comparator 110. The other end of the resistor 109 is connected to the drain of an N MOS FET 111 for inhibiting the comparator and the source of which is grounded. The drain of MOS FET 111 is connected to a point inside the comparator 111 the circuitry of which will be explained later in connection with Figure 15.

The output of the comparator 110 is connected to the set terminal S of the R—S flip-flop 112.

Various leads in Figure 12 are identified by letters and the wave forms appearing on these leads are shown in Figure 13 and identified by the same references.

When the Q output of flip-flop 100 is HIGH and that of NOR gate 101 is LOW, the output of NOR gate 104 becomes HIGH as does that of OR gate 107, MOS FET 118 becomes OFF, and MOS FET 119 becomes ON. Current accordingly flows in one direction through the coil 7 of the stepping motor. If the Q output of flip-flop 100 is LOW current flows in the opposite direction through the coil 7 through the ON MOS FET 114.

When a detection pulse $\emptyset$ appears at the terminal DP it is applied through inverter 120 to one input of NOR gate 105 the output of which becomes HIGH if the Q output of flip-flop 100 is HIGH and current flows through MOS FET 113, coil 7, MOS FET 115 and resistor 117 to ground, and a voltage drop is set up across said resistor 117. If the motor is in the condition of rotation and is able to be rotated by the normal drive pulse, a voltage drop across the resistor 117 as shown by the curve 151 of Figure 14 is produced during the 0.5 m sec. detection pulse. When, however, the detection pulse is applied, the voltage drop produced follows a curve as shown at 150 in Figure 14. The comparator compares the voltage applied to its positive terminal from the "live" end of the resistor 117 during a 0.5 m sec. detection pulse with that at the junction point of the resistors 108 and 109 and by suitably choosing the latter voltage, which in effect determines the threshold voltage of the comparator, the said comparator is caused to respond when the former voltage exceeds the threshold voltage and to provide a HIGH output signal when the condition of non-rotation exists.

When a HIGH output signal, due to the detection in this way of the condition of non-rotation of the motor, is produced at the output of the comparator 110 the RS flip-flop 112 is set and its Q output becomes HIGH and a correction drive pulse is applied to the motor which continues to be driven by these pulses so long as the condition of non-rotation exists. As will be seen the same action takes place when there is a LOW output from the flip-flop 100. Current consumption due to current

flowing through the resistors 108 and 109 is kept at a minimum because, owing to the action of MOS FET 111, which inhibits the comparator except during detection pulses, such current consumption does not occur except during said detection pulses. The economy of current consumption thus achieved will be apparent from Figure 14.

Figures 15 and 16 show a preferred construction for the comparator 110, which is constructed of CMOS elements, an important advantage enabling very compact integrated circuit construction to be employed. Figure 15 is a circuit diagram and Figure 16 is a block diagram representation.

In Figure 16 terminal 164 is the positive input terminal, terminal 165 is the negative input terminal, terminal 166 is the output terminal, and terminal 136 is an ENABLE terminal.

The functional performance of the comparator is shown in conventional manner by the following table:—

Positive Input	Negative Input	Enable Terminal	Output Terminal
—	—	0	—
V+>	V–	1	H
V+<	V–	1	L

Figure 15 shows the circuitry of the comparator. The positive terminal of the power supply (not shown) is connected *via* terminal 167 to the sources of two P MOS FETs 160 and 162. The gate and drain of MOS FET 160 are connected together and to the gate of MOS FET 162 and also to the drain of an N MOS FET 161 the gate of which is connected to terminal 169, and the source of which is connected to the drain of the N MOS FET 111. The drain electrode of MOS FET 162 is connected to the drain electrode of an N MOS FET 163 and also to the output terminal 166.

The gate of MOS FET 163 is connected to terminal 165, and the source thereof is connected to the source of MOS FET 161 and to the drain of MOS FET 111 the source of which is grounded. 136 is the ENABLE terminal and is connected to the gate of MOS FET 111. The characteristics of the N MOS FETs 160 and 162 are alike.

The MOS FET 124 is OFF when the ENABLE terminal 136 is LOW and the comparator is then inoperative. Said MOS FET 124 is ON when the terminal 136 is HIGH and the comparator is then operative. The voltage and current at the connection point 168 in Figure 15 become as shown in Figure 17 when an input voltage V_1 is applied at the terminal 164. In Figure 17 V_{168} is the voltage at point 168, and I_{168} is the current there.

The voltage at point 168 is applied to the gate of MOS FET 162, the saturation current of which is equal to I_{168}. Figure 18 shows the characteristics of the MOS FETs 162 and 163.

If the voltage V_2 applied to terminal 165 is larger than the gate/source voltage $V_{GS}=V_1$ of MOS FET 163 its saturated current becomes larger and the voltage V_{166} at the output terminal 166 becomes in the neighbourhood of LOW level. This condition is indicated at X in Figure 18.

If, however, $V_2<V_1$, the output V_{166} becomes HIGH. This condition is indicated at Y in Figure 18.

Referring once more to Figure 12 it will be seen that the voltage V across the detecting resistor 117 produced by the power supply voltage during a detection pulse is given by the equation:—

$$V=r/(R+r)[1-\mathrm{Exp}(-(R+r).t/L)]V_D$$

where R is the DC resistance of the coil 7, r is the resistance of the element 117, L is the effective inductance of the coil 7, t is the time taken to achieve saturation and V_D is the supply voltage. Due to the large increase in L when the condition of non-rotation occurs, the existence of this condition is easily detected by a logic threshold circuit with a threshold voltage so chosen with relation to V that it responds to provide a logic control output signal when V, as given by the above equation, is of a value which corresponds with the existence of the condition of non-rotation. If the threshold circuit employed is one having a threshold voltage V_{TH} which varies with the power supply voltage V_D the detection process will be insensitive to changes in the supply voltage V_D.

In the illustrated embodiment a CMOS inverter circuit is used in the circuitry for discrimination of the detection voltage. The threshold voltage of the inverter circuit is:

$$V_{TH}=[\alpha(V_D-V_{TP})+V_{TN}]/1+\alpha)$$

where the P MOS FET threshold voltage is V_{TP}, the N MOS FET threshold voltage is V_{TN}, the P-channel transistor scale value is Kp, the N-channel transistor scale value is KN, $\alpha=\sqrt{10/KN}$ and the power source voltage is V_D.

If $\alpha=V_{TP}/V_{TN}$, $V_{TH}=\alpha/(1+\alpha)$ and the threshold voltage V_{TH} of the CMOS inverter circuit will be proportional to the power supply voltage V_D. However, if these relations are not complied with—for example as a result of unavoidable variations in integrated circuit manufacture—strict proportionality is not obtained because the threshold voltages V_{TP}, V_{TN} differ from their intended values and the threshold voltage V_{TH} of the CMOS inverter circuit ceases to be proportional to the power supply voltage V_D, and the detection level accordingly changes with changes in the power supply voltage. However this defect is avoided in the illustrated embodiment because of the threshold voltage V_{TH} is changed with changes in the power supply voltage V_D, the said threshold voltage being obtained by means of a potentiometer (resistors 108, 109) which divide voltage V_D. In this way undesirable effects resulting from irregularity in integrated circuit manufacture are avoided and there is obtained a comparator which constitutes a logic circuit operating with a threshold voltage which is substantially independent of variations in supply voltage. Furthermore, by providing for variation in the voltage dividing potentiometer (resistors 108, 109) it is possible to set the threshold voltage accurately and thus avoid the necessity of having to have a close tolerance for the value of the detecting resistance 117 which can accordingly be chosen within an acceptably wide range of values.

In the particular embodiment of the invention hereinbefore described the normal drive pulse width was 3.9 m sec. and the correction drive pulse width was 7.8 m sec. These are typical practical figures. However, choice of the best pulse widths in a case in which a particular motor is to be used will be facilitated by a consideration of the current/pulse width and torque/pulse width curves of that motor. Such curves are exemplified by Figure 8. The normal drive pulse width, 0 to t_1 in Figure 1 should be chosen, with due regard to the general design specification of the motor, to be sufficient to produce reliable and stable operation of the motor when the load on it is only that necessary to drive the watch hands and the said normal pulses should be such as to secure maximum efficiency and minimum power consumption of the motor when operating against this load. The correction drive pulse width, i.e. the pulse width used when the condition of non-rotation exists, is 0—t_2 in Figure 8.

The illustrated embodiment has the advantages that it lends itself admirably to integrated circuit construction, is to a high degree insensitive to supply voltage changes operates accurately to discriminate between the conditions of rotation and non-rotation of the motor despite departures from intended values of circuit elements due to irregularities in the integrated circuit manufacture, is but little affected by temperature variations, does not require compliance with close tolerances in the values of the circuit elements employed and, being capable of large scale manufacture, is comparatively cheap to manufacture.

Attention is directed to our co-pending Applications Nos. 11988/78, 12486/78, 12487/78, 15440/78, 15441/78, 15666/78, 15667/78, 31910/78 and 46355/78, (Serial Nos. 1592893, 1592894, 1592895, 1592897, 1592898, 1592899, 1592900, 2005053 and 2009464), which describe related subject-matter.

WHAT WE CLAIM IS:—

1. An electronic timepiece as claimed in claim 1 of the parent specification No 47462/77, (Serial No. 1592892), including in a detection circuit for detecting whether the motor is in the condition of rotation or of non-rotation, a resistive detecting element in circuit with the drive coil of the motor so that the voltage drop across it is dependent on the effective inductance presented by said coil, there being provided a comparator for comparing said voltage drop with a reference voltage.

2. A timepiece as claimed in claim 1 wherein said reference voltage is provided by a potentiometer to which voltage from the power supply source of the timepiece

In the illustrated embodiment a CMOS inverter circuit is used in the circuitry for discrimination of the detection voltage. The threshold voltage of the inverter circuit is:

$$V_{TH}=[\alpha(V_D-V_{TP})+V_{TN}]/1+\alpha)$$

where the P MOS FET threshold voltage is V_{TP}, the N MOS FET threshold voltage is V_{TN}, the P-channel transistor scale value is Kp, the N-channel transistor scale value is KN, $\alpha=\sqrt{10/KN}$ and the power source voltage is V_D.

If $\alpha=V_{TP}/V_{TN}$, $V_{TH}=\alpha/(1+\alpha)$ and the threshold voltage V_{TH} of the CMOS inverter circuit will be proportional to the power supply voltage V_D. However, if these relations are not complied with—for example as a result of unavoidable variations in integrated circuit manufacture—strict proportionality is not obtained because the threshold voltages V_{TP}, V_{TN} differ from their intended values and the threshold voltage V_{TH} of the CMOS inverter circuit ceases to be proportional to the power supply voltage V_D, and the detection level accordingly changes with changes in the power supply voltage. However this defect is avoided in the illustrated embodiment because of the threshold voltage V_{TH} is changed with changes in the power supply voltage V_D, the said threshold voltage being obtained by means of a potentiometer (resistors 108, 109) which divide voltage V_D. In this way undesirable effects resulting from irregularity in integrated circuit manufacture are avoided and there is obtained a comparator which constitutes a logic circuit operating with a threshold voltage which is substantially independent of variations in supply voltage. Furthermore, by providing for variation in the voltage dividing potentiometer (resistors 108, 109) it is possible to set the threshold voltage accurately and thus avoid the necessity of having to have a close tolerance for the value of the detecting resistance 117 which can accordingly be chosen within an acceptably wide range of values.

In the particular embodiment of the invention hereinbefore described the normal drive pulse width was 3.9 m sec. and the correction drive pulse width was 7.8 m sec. These are typical practical figures. However, choice of the best pulse widths in a case in which a particular motor is to be used will be facilitated by a consideration of the current/pulse width and torque/pulse width curves of that motor. Such curves are exemplified by Figure 8. The normal drive pulse width, 0 to t_1 in Figure 1 should be chosen, with due regard to the general design specification of the motor, to be sufficient to produce reliable and stable operation of the motor when the load on it is only that necessary to drive the watch hands and the said normal pulses should be such as to secure maximum efficiency and minimum power consumption of the motor when operating against this load. The correction drive pulse width, i.e. the pulse width used when the condition of non-rotation exists, is $0—t_2$ in Figure 8.

The illustrated embodiment has the advantages that it lends itself admirably to integrated circuit construction, is to a high degree insensitive to supply voltage changes operates accurately to discriminate between the conditions of rotation and non-rotation of the motor despite departures from intended values of circuit elements due to irregularities in the integrated circuit manufacture, is but little affected by temperature variations, does not require compliance with close tolerances in the values of the circuit elements employed and, being capable of large scale manufacture, is comparatively cheap to manufacture.

Attention is directed to our co-pending Applications Nos. 11988/78, 12486/78, 12487/78, 15440/78, 15441/78, 15666/78, 15667/78, 31910/78 and 46355/78, (Serial Nos. 1592893, 1592894, 1592895, 1592897, 1592898, 1592899, 1592900, 2005053 and 2009464), which describe related subject-matter.

WHAT WE CLAIM IS:—

1. An electronic timepiece as claimed in claim 1 of the parent specification No 47462/77, (Serial No. 1592892), including in a detection circuit for detecting whether the motor is in the condition of rotation or of non-rotation, a resistive detecting element in circuit with the drive coil of the motor so that the voltage drop across it is dependent on the effective inductance presented by said coil, there being provided a comparator for comparing said voltage drop with a reference voltage.

2. A timepiece as claimed in claim 1 wherein said reference voltage is provided by a potentiometer to which voltage from the power supply source of the timepiece

is applied, whereby said reference voltage is caused to vary with the power supply source voltage.

3. A timepiece as claimed in claim 1 or 2 and comprising means for supplying to the detection circuit detection pulses of substantially shorter length than any of the drive pulses during intervals between successive drive pulses and means for bringing said detection circuit into operation only during said detection pulses.

4. A timepiece as claimed in claim 3 and comprising means for inhibiting the comparator except during the detection pulses.

5. A timepiece as claimed in any of the preceding claims and including means for producing normal drive pulses, correction drive pulses and detection pulses which are of widths respectively approximately equal to 3.9 m. sec, 7.8 m. sec and 0.5 m. sec.

6. A timepiece as claimed in any of the preceding claims wherein the comparator is a logic circuit with a threshold voltage determined by the reference voltage.

7. A timepiece as claimed in any of the preceding claims wherein the motor has a driving coil magnetically linked with a stator formed as a single integral body providing a saturable magnetic circuit and having a portion surrounding a permanently magnetised rotor with at least one pair of magnetic poles, the rest positions being positions in which a rotor diameter through opposite poles of a pair of each pair of rotor poles is angularly displaced with respect to a line in which lie opposite poles produced in the stator when a driving pulse is applied to the coil thereof.

8. A timepiece as claimed in claim 3 or 5 and comprising a crystal controlled time standard oscillator and a multi-stage flip-flop frquency divider driven thereby and wherein normal drive pulses, correction drive pulses and detection pulses are derived by combining wave forms taken from selected different stages of the frequency divider.

9. A timepiece as claimed in any of the preceding claims wherein the stepping motor is substantially as herein described with reference to Figures 4, 5 and 6 of the accompanying drawings.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
Lincoln House,
296—302 High Holborn,
London, WC1V 7JH.

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