

SYSTEM AND METHOD FOR THE VERIFICATION AND CHARACTERIZATION OF VLSI DEVICES**FIELD OF THE INVENTION**

[0001] The present invention relates to a system and method for the testing of semiconductor devices. More specifically, the present invention relates to a system and method for the verification and characterization of semiconductor devices, such as VLSI circuits using one or more on-chip networks of test probes.

BACKGROUND OF THE INVENTION

[0002] Semiconductor device manufacturers refer to Moore's Law to describe the ongoing reduction in size, and corresponding density increase, of semiconductor components such as transistors, interconnects, etc. on integrated circuits. Moore's Law states that roughly every two years, the number of transistors on an integrated circuit die (i.e. – a chip) will double.

[0003] To achieve this scale of increase, much technological effort is made to shrink the size of the components making up the integrated circuit. For example, Very Large Scale Integrated ("VLSI") circuits now have feature sizes of seven nanometers or less. Yet, despite the significant decreases in component sizes, the overall size (i.e. – die area) of many integrated circuits has still grown significantly, resulting in larger die sizes, as more features and capabilities are added to chips.

[0004] For example, the Apple M1 processor now used in some Apple devices reportedly has 11.8 billion transistors, and a die size of about 120 square mm, while the Apple M1Max processor reportedly has 57 billion transistors and a die size of about 490 square mm. Other advanced integrated circuits have similar or greater numbers of transistors and die sizes.

[0005] This combination of smaller components on larger dies poses many challenges to integrated circuit designers and manufacturers. In fact, a significant proportion of manufactured integrated circuits will not operate properly, or will not operate at a desired speed, due to a variety of factors, including: even minute undesired variations in the processes used to manufacture them; overly optimistic design rules employed in the software used to design the circuits resulting in deficient designs; circuit designer errors; etc.

[0006] Accordingly, the yield (the percentage of manufactured integrated circuits which operate within specified parameters of acceptance, as determined by post-manufacture testing) for the manufacture of these integrated circuits is typically lower than desired. In the

case of integrated circuits whose designs are at the limit of fabrication technologies, the yield can be much lower than is desired. Lower yields mean the manufacturer's profits are reduced and the supply of such advanced devices may be less than the demand. As Moore's law continues to push VLSI design limits even further, testing inadequacies and/or bottlenecks could prevent additional practical increases in chip densities and performance.

[0007] To ensure that they operate correctly, all integrated circuits must be tested after manufacture with the fundamental objective of the testing being to distinguish between good (properly operating) and faulty (one or more errors) integrated circuits.

[0008] It is desired to have a practical system and method for the verification and characterization of integrated circuits, such as VLSI devices or the like.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a novel system and method for the verification and characterization of semiconductor devices which obviates or mitigates at least one disadvantage of the prior art.

[0010] A VLSI semiconductor integrated circuit comprising: primary circuitry designed to perform required functions of the integrated circuit; at least one test network, manufactured on a plane over the primary circuitry and including transistors fabricated with BEOL and/or MOL processes, the transistors being selectively connectable by the test network to respective selected nodes of the primary circuitry to form on-chip test probes which are operable to allow the test network to connect respective transistors to corresponding nodes of the primary circuitry to apply an input and/or to observe an output at the selected nodes.

[0011] Preferably, the semiconductor integrated circuit includes a plurality of test networks, each operable to test respective portions of the primary circuitry.

[0012] According to another aspect of the present invention, there is provided a method of designing a VLSI semiconductor integrated circuit, comprising the steps of: (i) designing primary circuitry of the integrated circuit; (ii) determining a plurality of nodes corresponding to points within the primary circuitry where it is desired to apply test values and/or read test outputs to verify correct operation of the respective primary circuitry; and (iii) designing at least one test network, to be fabricated on a plane over the primary circuitry, to selectively connect

to respective ones of the determined nodes of the primary circuitry to enable the application of test signals to respective nodes and/or to receive test outputs from respective nodes.

[0013] According to yet another aspect of the present invention, there is provided a VLSI semiconductor integrated circuit comprising: primary circuitry implementing desired functions of the integrated circuit; and a test network fabricated on a plane over the primary circuitry, the test network operable to provide test probes to selected nodes of the primary circuitry to allow test values to be applied thereto and/or test outputs to be read therefrom.

[0014] The present invention provides a test network and method, implemented with BEOL and/or MOL devices, which provides on-chip test probes which, when activated, allow direct access to selected test points within circuits on an integrated circuit such as a VLSI chip, or when deactivated, are effectively removed from the circuits under test. The test network allows inputs to be directly applied to, and/or outputs to be directly observed at, test points of interest, greatly improving Observability and Controllability of the chip. Multiple test networks can be employed on a chip to allow circuits on the chip to be tested independently and/or in parallel. As the test circuitry and networks are implemented with BEOL and/or MOL devices, they can be manufactured on a separate plane of the chip, on one or more layers of the chip stacked atop the implemented primary circuits and thus do not require any significant increase in the chip's die area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 is a plot showing an historical trend in the increase in the average number of transistors per pin on VLSI integrated circuits;

Figure 2 is a schematic representation of a cross-point array test network to test primary circuitry nodes in accordance with an aspect of the present invention;

Figure 3 is a schematic representation of a prior art test flow; and

Figure 4 is a block level representation of a test flow in accordance with an aspect of the present invention;

Figure 5 is a schematic representation of a thirty two bit counter;

Figure 6 is a block diagram of the thirty two bit counter of Figure 5 when implemented

in accordance with an aspect of the present invention;

Figure 7 shows a block diagram of a Built In Self-Test system in accordance with an aspect of the present invention; and

Figure 8 shows a block diagram of another configuration of a Built In Self-Test system in accordance with an aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Previously, when integrated circuits were relatively less complex, functional testing was employed to characterize and verify operation of the integrated circuits. Functional tests are closely associated with the integrated circuit function and therefore, these tests are comparatively simple and straightforward when they are able to be employed. For example, a 4-bit binary counter can be exhaustively tested by applying $2^4 = 16$ test vectors, where each “test vector” corresponds to a possible one of the sixteen possible inputs and the corresponding correct outputs, by applying each test vector in turn and comparing the output generated to the corresponding one of expected “correct” outputs. However, as the complexity of integrated circuits increases, such functional testing quickly becomes impractical as the total set of possible inputs and corresponding correct outputs increases exponentially.

[0017] For example, an integrated circuit with thirty-two inputs has only a modest design complexity by today’s VLSI standards, but will require $2^{32} = 4,294,967,296$ test vectors for exhaustive functional testing. Even if these test vectors are applied at the rate of over one million test vectors per second, it will take well over an hour to test a single instance of this portion of the integrated circuit. Further, the time required for testing becomes much longer, and much more complex, if the integrated circuit contains sequential logic and/or as the amount of circuitry connected directly or indirectly to an input or output pin increases. Thus, it is clear that, due to their complexity, functional testing of VLSI circuits is impractical.

[0018] Figure 1, taken from the International Technology Roadmap for Semiconductors, shows this complexity from the test perspective. The figure illustrates the growing number, on average, of transistors per input and output (IO) pin for microprocessors (MPUs) and application specific integrated circuits (ASICs). The number of input and output pins (or pads) has not kept up with increases in integration and circuit complexity and this packaging

limitation puts severe additional constraints on the testing of complex ICs, such as VLSI devices.

[0019] Specifically, as mentioned above, the number of transistors on a chip continues to double approximately every two years. However, according to International Technology Roadmap for Semiconductors, the number of package pins grows at an annual rate of approximately 11%. Further exacerbating this issue, is the fact that typically, such larger, bigger integrated circuits require an increased number of pins to allow data flow to and from the integrated circuit. More pins are also required to provide adequate power and electrical grounds to the chip as power delivery and power supply noise are critical and limiting factors for the correct operation of high-performance integrated circuits.

[0020] Accordingly, approximately 50% of all pins on many modern VLSI circuits are dedicated to providing power and electrical grounds so as to deliver in excess of 100 watts of power to the billions of transistors in the VLSI chip and this rapid increase in the number of transistors per pin and the corresponding reduction in the number of pins available for other purposes, such as testing, exacerbates the difficulty in testing these chips.

[0021] Further complicating the matter is the fact that it is a widely accepted “rule of thumb” regarding testing that, for every one dollar testing costs at the chip level, it will cost ten dollars at the board level and will cost one hundred dollars at the system level to test, diagnose and replace the same defective integrated circuit. Therefore, chip manufacturers are well motivated to produce tested, high-quality devices at the lowest possible cost.

[0022] In a typical digital test scenario, a functional block (such as a counter, shift register, register, etc.) is tested by providing a sequence of Boolean inputs to the block and observing the outputs from the block. As a Figure of Merit (FOM), the concept of “Controllability” is defined as the difficulty to control a particular input signal to the block, while “Observability” is defined as the difficulty to observe a particular output signal of the block.

[0023] Often the difficulty of Controllability and Observability are measured in terms of the number of clock, or data, cycles required for the test sequence to execute before a particular desirable condition is realized to control, or observe, a node in the block. These cycles, and the defined inputs and expected outputs, form test vectors used to test the chips.

[0024] For example, if the output terminals of a counter “A” feed into a shift register “R”, then the input of shift register “R” can only be controlled through the count sequence of the

counter “A”. Similarly, the output of shift register “R” may only be visible at the output of the integrated circuit after passing through another, complex, logic block which may require another sequence of events or test vectors. Thus, modern VLSI circuits can have extremely high required numbers of test vectors and these high test vector counts lead to lower Controllability and Observability scores on the aforementioned FOM and significantly increase the cost of testing.

[0025] To address these challenges, semiconductor manufacturers have developed Design for Testability (DfT) strategies, such as Scan Chain and Built-in Self-Test (BIST), which are employed in attempts to reduce the high test-costs associated with testing and debugging at the sub-system and/or system level.

[0026] For example, Scan Chains include additional pins and circuitry on a VLSI chip to provide alternative pathways for test vectors to be applied to control and observe nodes on the chip, consequently reducing the test vector count, and hence the test cost.

[0027] A conventional BIST scheme, on the other hand, employs purpose-built additional circuitry on the chip to provide test sequences and expected responses and therefore can reduce the number of test vectors required to be applied from off chip through the I/O of the chip. However, even a BIST scheme can still require a large number of test vectors to test for all potential defects or imperfections.

[0028] Further, both Scan Chain and BIST implementations require purpose-built circuitry to be added to the chip die, undesirably increasing the die area. It is well known that the probability of a manufacturing fault increases exponentially as die sizes increase and thus there is a difficult tradeoff involved in increasing die area/size to improve testing capabilities.

[0029] The concept of Structural Testing became popular along with the DfT techniques. Structural Testing is different than Functional Testing in that it may not verify the functionality of the Device Under Test (“DUT”). Instead, it assumes that the manufacturing process can introduce defects or faults which need to be tested in an efficient manner. So, Structural Testing employs a fault model which becomes a basis for test generation and application.

[0030] For example, logic-level Stuck At Fault (“SAF”) models are one of the most popular fault models for Structural Testing. All SAFs are mapped onto the interconnects (or nets) between logic gates on the DUT, thus they are also referred to as stuck-line (“SL”) faults.

Under a fault condition, the affected line is assumed to have a permanent (stuck-at) logic “0” or “1” value that cannot be altered by input stimuli.

[0031] However, despite using these DfT techniques, the costs for test and verification of VLSI circuits have continued to escalate. Furthermore, most DfT techniques are intrusive and have a significant impact on integrated circuit’s design complexity, performance, power requirements and die area.

[0032] The present inventor has determined that new techniques are needed to provide improved Controllability and Observability, especially of critical, difficult to reach nodes in a VLSI circuit while ensuring that the integrated circuit’s native operation and die size is affected as little as possible.

[0033] Published PCT patent application WO 2023/285936 to Barlage et al., and assigned to the assignee of the present invention, teaches a thin film transistor (“TFT”) which is capable of being manufactured in Back End of Line (BEOL) and/or Middle of Line (“MOL”) processes. Published PCT patent application WO 2023/285951 to Barlage and Shoute, which is also assigned to the assignee of the present invention, teaches an Active Via, which is a via that can include a vertical implementation of one or more TFTs which can be formed in a BEOL or MOL process into a trans silicon via (“TSV”). The contents of these two published applications are incorporated herein, in their entirety, by reference. These BEOL and/or MOL devices can be formed in layers of a plane over conventional CMOS circuitry and thus do not utilize die area otherwise useful for the conventional circuitry and thus do not result in an increase of the die area of the integrated circuit.

[0034] Figure 2 illustrates a DfT scheme, in accordance with an aspect of the present invention, which employs an interconnected test network 100 of the above-mentioned BEOL and/or MOL TFTs and/or Active Vias 104 as test circuitry to act as on-chip test probes, allowing access to internal nodes of VLSI primary circuitry for test purposes.

[0035] In the example of Figure 2, the primary circuitry is digital circuitry (i.e. – logic, memory, etc.) but, as described further below, it is also contemplated that the present invention can also be applied to analog primary circuitry.

[0036] In the illustrated embodiment, test network 100 comprises N rows and M columns of a cross-point array. Network 100 further includes $M \times N$ BEOL and/or MOL devices 104_{1,1} to 104_{n,m} as shown.

[0037] As used herein, circuitry of the VLSI chip, such as logic, memory and/or analog circuits, which are implemented in Front End of Line manufacturing processes, such as with CMOS devices, is referred to as “primary circuitry”, while the additional circuitry implemented with the above-mentioned BEOL and/or MOL compatible processes is referred to as “test circuitry” and/or collectively as a “test network”.

[0038] As shown in Figure 2, each BEOL and/or MOL device 104 of the test circuitry is connected to a selected node 108 of interest of the primary circuitry such that Controllability and/or Observability can be achieved for those nodes 108. As discussed below, BEOL and/or MOL devices 104 and nodes 108 act as “on-chip test probes” for circuits on a VLSI chip.

[0039] In Figure 2, the source terminal of each BEOL and/or MOL device 104 in test network 100 is connected to a corresponding node $108_{1,1}$ to $108_{n,m}$ in the primary circuitry of an integrated circuit to be tested. The gate terminal of each BEOL and/or MOL device 104 is connected to a respective column line 112_1 to 112_m of network 100, while the drain terminal is connected to a respective row line 116_1 to 116_n . In the illustrated embodiment, the control signals for column lines 112 are provided by a register 120, but column lines 112 can be controlled in a variety of other manners, as desired, and as would be apparent to those of skill in the art.

[0040] Row lines 116 are connected to at least one register 124 and, in the illustrated embodiment, also to a second register 128. As described below, by having two registers (or equivalents) inputs to one or more nodes $108_{n,m}$ can be applied and/or outputs read from one or more nodes $108_{n,m}$ by network 100.

[0041] In use, one or more nodes 108 can be selected for test input (Controllability) and/or reading (Observability) by register 120 asserting the appropriate column line 112 and register 124 placing the desired test data on the corresponding row line 116. For example, a logic high can be applied to node $108_{2,2}$ by asserting column line 112_2 and asserting row line 116_2 .

[0042] Similarly, the value of a node 108 in the primary circuitry of the circuit under test can be read by asserting the corresponding column line 112 and reading the value on the corresponding row line 116. For example, the value of node $108_{1,2}$ can be read from row line 116_1 by register 128 after asserting column line 112_2 . As will be apparent to those of skill in the art, registers 120, 124 and 128 can be implemented in primary circuitry, if desired, or with BEOL and/or MOL devices.

[0043] In an example scenario wherein the behavior of a node, say $108_{1,1}$ needs to be observed, register 120 asserts high column line 112_1 enabling all BEOL and/or MOL devices $104_{n,1}$ connected to line 112_1 . The data on node $108_{1,1}$ drives the row 116_1 and register 128 captures its Boolean value.

[0044] As will be apparent, test network(s) 100 can allow for the simultaneously application of inputs to selected nodes 108 while also reading outputs from other nodes 108, but with some limitations. Specifically, the cross-point array of network 100 cannot simultaneously read and write to nodes 108 on the same row line 116 , nor can it write different values to nodes on the same row line 116 nor can it read values from two or more nodes 108 on the same row line.

[0045] Alternatively, a first test network 100 can be employed to write values (Controllability) to the primary circuitry under test and a second test network 100 can be employed to read output values from that same primary circuitry under test and thus the issues of simultaneous access to some rows and/or columns can be avoided.

[0046] As will now be apparent, network 100 enables the direct Controllability and/or Observability of selected nodes $108_{n,m}$ which otherwise could not be directly accessed for verification and/or characterization of the integrated circuit.

[0047] While not shown in Figure 2, it is also contemplated that register 120 can also include a column line with a system clock to provide precise timing control of the instance when a node is sampled. Further, the circuitry employed to write test values and read test results (registers 124 and 128 in the illustrated embodiment) can be programmed to drive the row lines or sense the data on row lines independently. In one scenario, a number of the row lines can be configured to sense the data on corresponding rows, while another number of row lines may be configured to drive or assert a particular data value on rows. The remaining number of row lines can be put into high impedance, to effectively remove them from the circuit under test, as desired.

[0048] Accordingly, while the example of Figure 2 shows network 100 implemented as a cross-point array, it is contemplated that more capable control networks can be implemented in network 100 as desired and the present invention is not limited to the use of a cross-point array.

[0049] Further, as mentioned above, it is contemplated that a VLSI circuit under test can have multiple instances of networks 100 implemented on the circuit to enable multiple circuit components and/or functions to be simultaneously, or independently, tested. For example, an arithmetic logic unit (ALU) can have a first network 100 dedicated to testing it, while a portion of the integrated circuit's output circuitry can have a second network 100 dedicated to testing it, etc. and/or networks 100 can be employed which only implement writing to nodes of interest or reading from nodes of interest. In fact, it is contemplated that VLSI circuits employing the present invention will have tens, or even hundreds, of instances of networks 100 employed on them and this is largely possible as test networks 100 are implemented with BEOL and/or MOL devices on planes above the primary circuitry, so they do not significantly increase die area.

[0050] In the case where the primary circuitry is analog, inputs to nodes 108 from test network 100 can be provided from a digital to analog converter, or from analog circuitry, and outputs from nodes 108 can be applied to analog to digital converters, or analog circuitry, as desired.

[0051] As will now be apparent to those of skill in the art, the present invention provides on-chip test networks implementing test probes providing Observability and/or Controllability of selected nodes of the primary circuitry.

[0052] As mentioned, networks 100 are implemented with BEOL and/or MOL devices. Therefore networks 100 can be formed in a stacked manner, wherein one or more networks 100 can be formed over one or more other networks 100, which are in turn all formed over the primary circuitry of the chip, without increasing the die area of the chip. In such a case, devices 104 in a layer connect to respective nodes 108 of the primary circuitry through vias which can pass through interposed layers of test circuitry in addition to layers of the primary circuitry.

[0053] In a presently preferred embodiment, only n-type BEOL and/or MOL devices 104 are used in network 100 which could affect the propagation of a logic high signal through BEOL and/or MOL devices 104. As a mitigation feature, row lines 116_n can be pre-charged to logic high from the register 124, 128. Once the desired test output data is captured in register 124 or 128, it can be scanned out through the I/O pins or pads on the chip under test.

[0054] Similarly, the value of one or more nodes in the primary circuitry of a DUT can be controlled through network 100. For example, data can be asserted from register 124 when a row line 116_n is activated. After a defined delay, a particular column line, say line 112₁, is

enabled and, under these circumstances, the test data is driven to appropriate nodes in the DUT. A DUT node 108 that is being controlled should be designed to accept the data through network 100 without creating a logical conflict.

[0055] As mentioned above, in a typical situation, networks 100 can be manufactured in a BEOL and/or MOL process over conventional CMOS, or any other type of primary logic on a VLSI chip, etc. and merely require an additional subset of masks to facilitate testing of the VLSI chip, or Device Under Test (DUT). While it is contemplated that it may be desired that some of the control circuitry for network 100 be implemented in the primary circuitry of the chip, generally networks 100 do not result in a significant increase in die area as the bulk of network(s) 100 is in additional planes of layers formed over the primary circuitry.

[0056] It is contemplated that the present invention therefore provides significant advantages in that chip designers can achieve greatly enhanced Controllability and Observability of their designs without affecting their design processes or procedures, as direct test access is provided to and from nodes within their circuit designs.

[0057] Figure 3 shows a schematic representation of prior art test flows. A set of test vectors 200 is applied to a DUT 204 to obtain a set of test results 208, which are then compared to an expected set of outputs. If DUT 204 contains sequential logic, such as a sixteen bit counter at the input and a twenty four bit counter at the output, the application of test vectors 200 would require 2^{16} (65,536) times 2^{24} (16,777,216) = 1,099,511,627,776 test steps to verify.

[0058] Figure 4 shows a schematic representation of a test flow in accordance with an aspect of the present invention. In Figure 4, a DUT 300 comprises the primary circuitry 304, implemented in CMOS or the like, and one or more test networks 308, implemented with BEOL and/or MOL devices 104, as described above and in accordance with the present invention. A set of test vectors 312 are applied to test networks 308 which apply the corresponding test values to appropriate nodes in primary circuitry 304 and which read corresponding output values from appropriate nodes of primary circuitry 304 to obtain a set of test results 316.

[0059] As will now be apparent to those of skill in the art from the discussion above, the set of test vectors 312 can be much smaller (and accordingly much faster to process) than a set of test vectors required to test a similar DUT with prior art techniques as test signals can be applied directly to nodes of interest in the primary circuitry without having to step upstream circuitry through states which would otherwise be necessary to apply the desired test input to

a node under test. Specifically, in the example above, each of the sixteen bit counter and the twenty four bit counter can be tested separately and, if desired, in parallel, to greatly reduce the time required to test the circuit. Also, if more than one network 100 is present on DUT 300, test vectors can be applied and results read in parallel further reducing test and verification times.

[0060] Figure 5 shows a block diagram of thirty-two bit counter 400 which has a clock input (CLK), an Enable input 404 and a logic output 408, such that counter 400 increments on each clock cycle when the Enable signal is high. In a conventional test regime, counter 400 would require $2^{32} = 4,294,967,296$ test vectors/clock cycles.

[0061] Figure 6 shows a block diagram of counter 400 implemented in accordance with an aspect of the present invention. The circuit designer of counter 400 has implemented counter 400 as a set of three, serially-connected, logic blocks comprising: a first twelve bit counter 425; a second twelve bit counter 427; and a third eight bit counter 429 to form the thirty two bit counter.

[0062] In the example, by using network 100, the output of counter logic block 425 can be observed at node $108_{1,1}$, the output of counter block 427 can be observed at node $108_{2,1}$ and the output of counter logic block 429 can be observed at node $108_{3,1}$.

[0063] Similarly, by using network 100, an input to counter logic block 425 can be applied at node $108_{1,2}$, an input to logic counter block 427 can be applied at node $108_{2,2}$ and an input to counter logic block 429 can be applied at node $108_{3,2}$.

[0064] Thus, instead of requiring $2^{32} = 4,294,967,296$ test vectors/clock cycles to test, counter 400 requires $2^{12} + 2^{12} + 2^8 = 4096 + 4096 + 256 = 8,448$ test vectors/clock cycles to test. Further, if nodes $108_{1,1}$, $108_{1,2}$ and $108_{1,3}$ are connected to separate networks 100, counter 400 can be tested in parallel in $2^{12} = 4096$ clock cycles.

[0065] In the example of Figure 6, to prevent a logic input conflict when applying inputs from network 100 to nodes of the primary circuitry, muxes 431, 433 and 435 are employed. Each mux 431, 433 and 435 is a two to one mux and has a mux control line, 437, 439 and 441 respectively, which is used to select whether an Enable input from the primary circuitry or a test input from network 100 is applied to the respective circuit. Appropriate signals for mux control lines 437, 439 and 441 can be provided from network 100, or from the primary circuitry or from a combination of both.

[0066] While the two to one muxes can be omitted if the primary circuitry employs tri-state logic to prevent conflicts when applying test vector inputs via network 100, the use of muxes is currently preferred as it enables test vectors for the circuit blocks to be applied in parallel. For example, as mentioned above, each of counters 425, 427 and 429 can be tested independently of one another as the inputs and outputs of each can be directly controlled and observed.

[0067] As will now be apparent, both Controllability and Observability of primary circuitry such as counter 400 are greatly improved by the use of the present invention. A circuit designer can include one or more test networks 100 on the semiconductor chip being designed to provide direct Control and Observability at significant nodes in the chip's circuitry to greatly reduce test times and the complexity of test vectors. By implementing networks 100 with BEOL and/or MOL devices, no significant increase of die area is required for the test circuitry.

[0068] As discussed, the designer of a VLSI chip can employ multiple networks 100 to allow various functions and circuit areas of the chip to be tested independently of one another and/or in parallel. Networks 100 can be employed to test a chip for manufacturing defects, but can also be employed with BIST strategies to allow devices to be regularly tested and verified as they age over their lifetime. Such BIST functions can provide an alarm, or notice, to the system in which the chip is installed if a fault is detected.

[0069] As is known, in addition to testing after manufacture, BIST functions can also be employed to test the DUT over its lifetime, and help in taking remedial actions. For example, if a fault is detected in a circuit on the chip when the chip is operating at its operational clock speed, but the fault does not occur at a lower clock speed, the operational clock speed can be degraded by the system to one where the chip operates correctly. Similarly, if errors are determined in a core of a multi-core processor chip, the core with the fault can be disabled by the system. Such BIST-type functionality can employ appropriate test vectors that are executed on each power-up event of the integrated circuit, or at intervals otherwise specified by the circuit designer.

[0070] A first example of a BIST system 700 in accordance with an aspect of the present invention is shown in Figure 7. The device under test (DUT) 704, which is typically formed on the conventional CMOS layer of the integrated circuit, can be a functional subset of the

integrated circuit such as an ALU, a memory or an Integer Core, or can be the entire integrated circuit.

[0071] BIST system 700 includes a largely conventional BIST controller 708 that controls the overall test operation to produce a “Pass / Fail” output 712 which can be used by a system controller, or other management device, on the integrated circuit to take appropriate error mitigation steps, or to deactivate a defective DUT 704, or functional block (such as a computation core) on DUT 704, etc.

[0072] BIST controller 708 receives a system clock 716 and inputs from the integrated circuit system controller or other system to start the test process when deemed necessary and outputs “pass or fail” test responses at the conclusion of the test. A set of appropriate test vectors 720 comprising test inputs and expected corresponding outputs, in a typical scenario, are stored in a non-volatile, read only memory (ROM) or alternatively, test vectors 720 can be provided using a Linear Feedback Shift Register (LFSR) which is capable of generating pseudo-random test sequences. An LFSR typically consists of digital logic and can be implemented with CMOS transistors and the design of such functional blocks is well known.

[0073] Test vectors 720 are applied to DUT 704 via network 724, which is a test network such as network 100 described above, to achieve Controllability of DUT 704. In the illustrated example, network 724 also provides Observability of DUT 704 by providing corresponding results of the applied test vectors to a response analyzer 728, which compares the results to expected outputs for the corresponding test vectors 720 and provides the results of those comparisons to BIST controller 708.

[0074] Test operation starts with BIST controller 708 receiving a signal 718 to start the test. BIST controller 708 puts DUT 704 in a test mode so it can accept the test vectors 720, and it enables the test vectors 720 to be applied to DUT 704 through test network 724.

[0075] Test vectors 720 are applied sequentially to DUT 704 through test network 724 and the corresponding responses from DUT 704 are compared to the expected responses by response analyzer 728, with the results of the comparisons being communicated to BIST controller 708. BIST controller 708 then asserts an output 712 signifying DUT 704 has passed or failed the test or tests.

[0076] Figure 8 shows another example of a BIST system 760 in accordance with an aspect of the present invention. In Figure 8, like components to those of system 700 of Figure

7 are indicated with like reference numerals. In system 760, instead of test network 724, which operated bi-directionally to both apply test vectors and to obtain corresponding results, BIST system 760 employs a Controllability test network 764 to apply test vectors 720 and an Observability test network 768 to obtain test results. Test networks 764 and 768 are networks such as test network 100 described above, each of which is implemented as a unidirectional network, with network 764 operating to apply test signals and network 768 operating to receive test results.

[0077] A method of employing one embodiment of the present invention can comprise the chip designer designing the primary circuitry for a VLSI, substantially in a conventional manner. The designer then selects nodes, functional blocks, etc. within the primary circuitry where it is desired, for test purposes, to have Controllability and/or Observability. The designer then designs at least one test network to provide an on-chip test probe for each of nodes selected within the primary circuitry. The completed design is then manufactured by first manufacturing the primary logic and then by forming, with BEOL and/or MOL processes, the at least one test network of BEOL and/or MOL transistors atop the primary logic, with vias formed to connect the BEOL and/or MOL transistors of the test networks to the corresponding selected nodes of the primary logic, to obtain the desired on-chip test probes which can be used to initially test for manufacturing faults and/or to serve as BIST test points.

[0078] As will now be apparent, the present invention provides on chip test probes which enable direct access to selected node test points within primary circuitry on a VLSI chip. One or more test networks, implemented using BEOL and/or MOL devices, provide on-chip test probes which allow inputs to be directly applied to, and outputs to be directly observed at, selected nodes of interest in the primary circuitry, greatly improving Observability and Controllability of the primary circuitry of the chip. Multiple test networks can be employed on a chip to allow different circuits of the primary circuitry on the chip to be tested independently and/or in parallel and/or in an ongoing, BIST-type, manner.

[0079] As the test circuitry and networks are implemented with BEOL and/or MOL devices, they can be manufactured on planes of layers of the chip stacked atop the primary circuitry and thus do not require any significant increase in the chip's die area.

[0080] The above-described embodiments of the invention are intended to be examples of the present invention and alterations and modifications may be effected thereto, by those of

skill in the art, without departing from the scope of the invention which is defined solely by the claims appended hereto.

We claim:

1. A VLSI semiconductor integrated circuit comprising:
primary circuitry designed to perform required functions of the integrated circuit;
at least one test network, manufactured on a plane over the primary circuitry and including transistors fabricated with BEOL and/or MOL processes, the transistors being selectively connectable by the test network to respective selected nodes of the primary circuitry to form on-chip test probes which are operable to allow the test network to connect respective transistors to corresponding nodes of the primary circuitry to apply an input and/or to observe an output at the selected nodes.
2. The VLSI semiconductor integrated circuit of claim 1 wherein the at least one test network includes at least one shift register to select transistors to connect to corresponding selected nodes.
3. The VLSI semiconductor integrated circuit of claim 2 wherein the at least one test network includes at least a second shift register to apply test inputs to the selected transistors connected to the corresponding selected nodes.
4. The VLSI semiconductor integrated circuit of claim 1 wherein the test network comprises a cross-point array.
5. The VLSI semiconductor integrated circuit of claim 2 further including an analog to digital converter to convert analog test signals received from an on-chip test probe to digital values.
6. The VLSI semiconductor integrated circuit of claim 1 wherein transistors of the test network connect to the selected nodes of the primary circuitry through vias.
7. The VLSI semiconductor integrated circuit of claim 1 further including a plurality of test networks, each test network being operable to test a different portion of the primary

circuitry.

8. The VLSI semiconductor integrated circuit of claim 7 wherein the plurality of test networks can operate to test the respective different portions of the primary circuitry in parallel.

9. The VLSI semiconductor integrated circuit of claim 1 wherein the at least one test network tests the primary circuitry on each power up of the primary circuitry.

10. The VLSI semiconductor integrated circuit of claim 1 further comprising a built in self test controller, a source of test vectors for the primary circuitry, a source of test vector expected results and wherein the built in self test controller operates to apply test vectors from the test vector source to the primary circuitry and to obtain and compare corresponding results from the primary circuitry for the applied test vectors and to determine and output a corresponding signal representing a pass or fail for the primary circuitry's execution of the applied test vectors.

11. The VLSI semiconductor integrated circuit of claim 10 wherein the built in self test controller tests the integrated circuit upon each instance of the circuit being energized.

12. The VLSI semiconductor integrated circuit of claim 10 wherein the built in self test controller tests the integrated circuit upon receiving from the primary circuitry an instruction to perform a test.

13. The VLSI semiconductor circuit of claim 7 wherein different test networks test different functional blocks of the semiconductor integrated circuit.

14. A method of designing a VLSI semiconductor integrated circuit, comprising the steps of:

- (i) designing primary circuitry of the integrated circuit;
- (ii) determining a plurality of nodes corresponding to points within the primary circuitry

where it will be desired to apply test values and/or read test outputs to verify correct operation of the respective primary circuitry; and

(iii) designing at least one test network, to be fabricated on a plane over the primary circuitry, to selectively connect to ones of the respective determined nodes of the primary circuitry to enable the application of test signals to respective nodes and/or to receive test outputs from respective nodes.

15. The method of claim 14 wherein the at least one test network is a cross-point array.

16. The method of claim 14 wherein the primary circuitry includes a plurality of functional blocks and wherein each functional block has a corresponding test network.

17. A VLSI semiconductor integrated circuit comprising:

primary circuitry implementing desired functions of the integrated circuit; and
a test network fabricated on a plane over the primary circuitry, the test network operable to provide test probes to selected nodes of the primary circuitry to allow test values to be applied thereto and/or test outputs to be read therefrom.