What is claimed is:

1. A semiconductor device comprising:

a semiconductor die including a central region comprising a semiconductor integrated circuit and a peripheral region surrounding the central region, wherein the peripheral region comprises a left-bottom corner region, a left-upper corner region, a right-upper corner region and a right-bottom corner region;

a defect detection structure in the peripheral region, the defect detection structure comprising a first conduction loop in the left-bottom corner region, a second conduction loop in the right-bottom corner region, a third conduction loop in the left-bottom corner region and the left-upper corner region and a fourth conduction loop in the right-bottom corner region and the right-upper corner region; and

an input-output circuit electrically connected to respective end nodes of the first conduction loop, the second conduction loop, the third conduction loop and the fourth conduction loop.

2. The semiconductor device of claim 1, wherein the end nodes of the first, second, third, and fourth conduction loops are in an end node region between the left-bottom corner region and the right-bottom corner region.

3. The semiconductor device of claim 1 or claim 2, wherein the first, second, third and fourth conduction loops have a common input end node.

4. The semiconductor device of any one of claims 1 to 3, wherein the first conduction loop extends along the peripheral region from an input end node in an end node region between the left-bottom corner region and the right-bottom corner region to a first

edge region between the left-bottom corner region and the left-upper corner region and returns from the first edge region to a first output end node of the end nodes in the end node region,

wherein the second conduction loop extends along the peripheral region from the input end node to a second edge region between the right-bottom corner region and the right-upper corner region and returns from the second edge region to a second output end node of the end nodes in the end node region,

wherein the third conduction loop extends along the peripheral region from the input end node to a third edge region between the left-upper corner region and the right-upper corner region and the left-upper corner region and returns from the third edge region to a third output end node of the end nodes in the end node region,

wherein the fourth conduction loop extends along the peripheral region from the input end node to the third edge region and the right-upper corner region and returns from the third edge region to a fourth output end node of the end nodes in the end node region, and

wherein existence of defects in the semiconductor die and locations of the defects are based on first, second, third, and fourth test output signals at the first, second, third, and fourth output end nodes.

5. The semiconductor device of claim 4,

wherein a horizontal line of the first conduction loop extending from the input end node to the first edge region overlaps with a portion of a horizontal line of the third conduction loop extending from the input end node to the third edge region, and

wherein a horizontal line of the second conduction loop extending from the input end node to the second edge region overlaps with a portion of a horizontal line of the fourth

conduction loop extending from the input end node to the third edge region.

6. The semiconductor device of any one of claims 1 to 5, wherein the defect detection structure is in a plurality of conduction layers comprising a ring-shaped three-dimensional structure surrounding the central region.

7. The semiconductor device of any one of claims 1 to 3, wherein the first conduction loop and the second conduction loop are in a first conduction layer and a second conduction layer, and the third conduction loop and the fourth conduction loop are in the first conduction layer and a third conduction layer.

8. The semiconductor device of claim 7, wherein the defect detection structure comprises:

a first horizontal line in the first conduction layer, wherein the first horizontal line comprises a ring shape extending along the peripheral region in the left-bottom corner region, the left-upper corner region, the right-upper corner region and the right-bottom corner region, and wherein the first horizontal line is discontinuous in a third edge region between the left-upper corner region and the right-upper corner region;

a second horizontal line in the second conduction layer, the second horizontal line extending from a first output end node of the end nodes in an end node region between the left-bottom corner region and the right-bottom corner region to a first edge region between the left-bottom corner region and the left-upper corner region;

a third horizontal line in the second conduction layer, the third horizontal line extending from a second output end node of the end nodes in the end node region to a second edge region between the right-bottom corner region and the right-upper corner

region;

a fourth horizontal line in the third conduction layer, the fourth horizontal line extending from a third output end node of the end nodes in the end node region to the third edge region;

a fifth horizontal line in the third conduction layer, the fifth horizontal line extending from a fourth output end node of the end nodes in the end node region to the third edge region;

a first vertical line connecting the first horizontal line and the second horizontal line in the first edge region;

a second vertical line connecting the first horizontal line and the third horizontal line in the second edge region;

a third vertical line connecting the first horizontal line and the fourth horizontal line in the third edge region; and

a fourth vertical line connecting the first horizontal line and the fifth horizontal line in the third edge region.

9. The semiconductor device of any one of claims 1 to 3, wherein the first conduction loop and the second conduction loop are in a first conduction layer, and the third conduction loop and the fourth conduction loop are in the first conduction layer and a second conduction layer.

10. The semiconductor device of claim 9, wherein the defect detection structure comprises:

a first horizontal line in the first conduction layer, wherein the first horizontal line comprises a ring shape extending along the peripheral region in the left-bottom corner

region, the left-upper corner region, the right-upper corner region and the right-bottom corner region, and wherein the first horizontal line is discontinuous in a third edge region between the left-upper corner region and the right-upper corner region;

a second horizontal line in the first conduction layer, wherein the second horizontal line extends from a first output end node of the end nodes in an end node region between the left-bottom corner region and the right-bottom corner region to a first edge region between the left-bottom corner region and the left-upper corner region and connected to the first horizontal line in the first edge region;

a third horizontal line in the first conduction layer, wherein the third horizontal line extends from a second output end node of the end nodes in the end node region to a second edge region between the right-bottom corner region and the right-upper corner region and connected to the first horizontal line in the second edge region;

a fourth horizontal line in the second conduction layer, wherein the fourth horizontal line extends from a third output end node of the end nodes in the end node region to a third edge region;

a fifth horizontal line in the second conduction layer, wherein the fifth horizontal line extends from a fourth output end node of the end nodes in the end node region to the third edge region;

a first vertical line connecting the first horizontal line and the fourth horizontal line in the third edge region; and

a second vertical line connecting the first horizontal line and the fifth horizontal line in the third edge region.

11. The semiconductor device of any one of claims 1 to 3, wherein the first conduction loop and the second conduction loop are in a first conduction layer, and the third

conduction loop and the fourth conduction loop are in a second conduction layer.

12. The semiconductor device of claim 11, wherein the defect detection structure comprises:

a first horizontal line in the first conduction layer, the first horizontal line extending from a first edge region between the left-bottom corner region and the left-upper corner region to a second edge region between the right-bottom corner region and the right-upper corner region;

a second horizontal line in the first conduction layer, the second horizontal line extending from a first output end node of the end nodes in an end node region between the left-bottom corner region and the right-bottom corner region to the first edge region in the left-bottom corner region and connected to the first horizontal line in the first edge region;

a third horizontal line in the first conduction layer, the third horizontal line extending from a second output end node of the end nodes in the end node region to the second edge region in the right-bottom corner region and connected to the first horizontal line in the second edge region;

a fourth horizontal line in the second conduction layer, the fourth horizontal line comprising a ring shape extending along the peripheral region in the left-bottom corner region, the left-upper corner region, the right-upper corner region and the right-bottom corner region, wherein the fourth horizontal line is discontinuous in a third edge region between the left-upper corner region and the right-upper corner region;

a fifth horizontal line in the second conduction layer, the fifth horizontal line extending from a third output end node of the end nodes in the end node region to the third edge region in the left-bottom corner region and the left-upper corner region and connected to the fourth horizontal line in the third edge region;

a sixth horizontal line in the second conduction layer, the sixth horizontal line extending from a fourth output end node of the end nodes in the end node region to the third edge region in the right-bottom corner region and the right-upper corner region and connected to the fourth horizontal line in the third edge region; and

a vertical line connecting the first horizontal line and the fourth horizontal line in the end node region.

13. The semiconductor device of any one of claims 1 to 12, wherein the input-output circuit comprises:

an output pad; and

a selection circuit configured to connect the output pad sequentially to a first output end node of the first conduction loop, a second output end node of the second conduction loop, a third output end node of the third conduction loop and a fourth output end node of the fourth conduction loop.

14. The semiconductor device of any one of claims 1 to 13,

wherein the semiconductor device comprises a plurality of semiconductor dies stacked in a vertical direction, and

wherein the defect detection structure comprises a ring-shaped three-dimensional structure in a plurality of conduction layers respectively included in the plurality of semiconductor dies.

15. A defect detection structure in a peripheral region of a semiconductor die surrounding a central region of the semiconductor die comprising a semiconductor integrated circuit, the defect detection structure comprising:

a first conduction loop in a left-bottom corner region of the peripheral region;

a second conduction loop in a right-bottom corner region of the peripheral region;

a third conduction loop in the left-bottom corner region and a left-upper corner region of the peripheral region; and

a fourth conduction loop in the right-bottom corner region and a right-upper corner region of the peripheral region.

16. A method of detecting defects in a semiconductor die including a central region comprising a semiconductor integrated circuit and a peripheral region surrounding the central region, the peripheral region including a left-bottom corner region, a left-upper corner region, a right-upper corner region and a right-bottom corner region, the method comprising:

forming a defect detection structure in the peripheral region, the defect detection structure comprising a first conduction loop in the left-bottom corner region, a second conduction loop in the right-bottom corner region, a third conduction loop in the left-bottom corner region and the left-upper corner region and a fourth conduction loop in the right-bottom corner region and the right-upper corner region;

applying a test input signal to an input end node of the defect detection structure;

receiving respective first, second, third, and fourth test output signals from first, second, third, and fourth output end nodes of the first, second, third and fourth conduction loops; and

determining existence of defects in the semiconductor die and locations of the defects based on the test input signal and the first, second, third, and fourth test output signals.

17. The method of claim 16, wherein the first, second, third, and fourth test output signals are provided sequentially through one output pad.

18. The method of claim 16, wherein at least two of the first, second, third, and fourth test output signals are provided in parallel through at least two output pads.

19. The method of any one of claims 16 to 18, wherein the locations of the defects are determined by comparing a delay time of the first test output signal and a delay time of the second test output signal.

20. The method of any one of claims 16 to 19, wherein the locations of the defects are determined by comparing a delay time of the third test output signal and a delay time of the fourth test output signal.