CLAIMS

1. A control method, applied to a semiconductor memory, the semiconductor memory comprising a Data Mask (DM) pin, the DM pin being configured to receive an input mask signal for write data, the method comprising:

in response to that the semiconductor memory is in a preset test mode, controlling, when a fourth Operand (OP) in a first Model Register (MR) is in a first state, an impedance of the DM pin to be a first value according to a third OP in a third MR; or

controlling, when the fourth OP in the first MR is in a second state, the impedance of the DM pin to be a second value;

wherein the fourth OP is configured to indicate whether to enable the DM pin, and the third OP is configured to indicate whether the DM pin is a test object in the preset test mode.

2. The control method according to claim 1, wherein the first value comprises a first impedance parameter or a second impedance parameter, and the first state indicates to enable the DM pin; controlling the impedance of the DM pin to be the first value according to the third OP in the third MR comprises:

controlling, when the third OP is in a third state, the impedance of the DM pin to be the first impedance parameter according to a first OP in the first MR, the third state indicating that the DM pin is the test object in the preset test mode;

controlling, when the third OP is in a fourth state, the impedance of the DM pin to be the second impedance parameter according to a second OP in a second MR, the fourth state indicating that the DM pin is not the test object in the preset test mode;

wherein the semiconductor memory further comprises at least one data pin, the data pin is configured to receive or output data, the first OP is configured to indicate that an impedance of the at least one data pin in an output driver state is the first impedance parameter, and the second OP is configured to indicate that the impedance of the at least one data pin in a termination state is the second impedance parameter.

3. The control method according to claim 2, wherein the second value comprises a high impedance state, the second state indicates not to enable the DM pin; controlling the impedance of the DM pin to be the second value comprises:

controlling the DM pin to be in the high impedance state through a first fixed level signal.

4. The control method according to claim 3, wherein the method further comprises:

acquiring the first OP and the fourth OP stored in the first MR, the second OP stored in the second MR, and the third OP stored in the third MR;

decoding the third OP and the fourth OP respectively to obtain a first test flag signal and an enable control signal; and

in response to that the semiconductor memory is in the preset test mode, selecting, in a case where the enable control signal is in a first level state, the first OP or the second OP to control the impedance of the DM pin according to a level state of the first test flag signal; or controlling, in a case where the enable control signal is in a second level state, the DM pin to be in the high impedance state through the first fixed level signal;

wherein when the fourth OP is in the first state, the enable control signal is in the first level state; when the fourth OP is in the second state, the enable control signal is in the second level state; when the third OP is in the third state, the first test flag signal is in the first level state; and when the third OP is in the fourth state, the first test flag signal is in the second level state.

5. The control method according to claim 4, wherein the method further comprises:

determining a first non-test mode control signal and a second impedance control signal;

in response to that the semiconductor memory is in the preset test mode, outputting, based on one of the first fixed level signal, the first OP and the second OP, a first impedance

control signal according to the level state of the first test flag signal and the level state of the enable control signal; or in response to that the semiconductor memory is not in the preset test mode, outputting, based on the first non-test mode control signal, the first impedance control signal; and

selecting one of the first impedance control signal and the second impedance control signal to control the impedance of the DM pin according to a working state of the semiconductor memory;

wherein the first non-test mode control signal is configured to indicate an impedance of the DM pin in a mode except the preset test mode, and the second impedance control signal is configured to indicate an impedance of the data pin in the output driver state; or the first non-test mode control signal is configured to indicate the impedance of the data pin in the output driver state, and the second impedance control signal is configured to indicate the impedance of the DM pin in a mode except the preset test mode.

6. The control method according to claim 4 or 5, wherein the preset test mode refers to a Package Output Driver Test Mode (PODTM), and the PODTM is configured to test the impedance of the DM pin or the at least one data pin after packaging;

a standard number of the first MR is 5, the first OP refers to an OP from a second bit to a first bit stored in the first MR, and the fourth OP refers to an OP at a fifth bit stored in the first MR; a standard number of the second MR is 34, and the second OP refers to an OP from a second bit to a 0th bit stored in the third MR; a standard number of the third MR is 61, and the third OP refers to an OP from a 4th bit to a 0th bit stored in the third MR; and

the first level state is a high level state, and the second level state is a low level state.

7. A semiconductor memory, comprising a Data Mask (DM) pin, a first Model Register (MR), a third MR, and a first driver circuit, the first driver circuit being connected with the first MR, the third MR and the DM pin respectively; wherein

the DM pin is configured to receive an input mask signal for write data;

the first driver circuit is configured to, in response to that the semiconductor memory is in a preset test mode, control, when a fourth Operand (OP) in the first MR is in a first state, an impedance of the DM pin to be a first value according to a third OP in the third MR; or

control, when the fourth OP in the first MR is in a second state, the impedance of the DM pin to be a second value;

wherein the fourth OP is configured to indicate whether to enable the DM pin, and the third OP is configured to indicate whether the DM pin is a test object in the preset test mode.

8. The semiconductor memory according to claim 7, wherein the semiconductor memory further comprises a second MR, and the second MR is connected with the first driver circuit; the first value comprises a first impedance parameter or a second impedance parameter, and the second value refers to a high impedance state;

the first driver circuit is specifically configured to control, in a case where the fourth OP is in the first state and the third OP is in a third state, the impedance of the DM pin to be the first impedance parameter according to a first OP in the first MR; or

control, in a case where the fourth OP is in the first state and the third OP is in a fourth state, the impedance of the DM pin to be the second impedance parameter according to a second OP in the second MR; or

control, in a case where the fourth OP is in the second state, the impedance of the DM pin to be in a high impedance state according to a first fixed level signal;

wherein the first state indicates to enable the DM pin, and the second state indicates not to enable the DM pin; the third state indicates that the DM pin is the test object in the preset test mode, and the fourth state indicates that the DM pin is not the test object in the preset test mode; the semiconductor memory further comprises at least one data pin, the data pin is configured to receive or output data, the first OP is configured to indicate that an impedance of the at least one data pin in an output driver state is the first impedance parameter, and the second OP is configured to indicate that an impedance of the at least one data pin in a termination state is the second impedance parameter.

9. The semiconductor memory according to claim 8, wherein the semiconductor memory further comprises a first decoding module and a second decoding module; wherein

the first MR is configured to store and output the first OP and the fourth OP;

the second MR is configured to store and output the second OP;

the third MR is configured to store and output the third OP;

the first decoding module is configured to receive the third OP, decode the third OP and output a first test flag signal;

the second decoding module is configured to receive the fourth OP, decode the fourth OP and output an enable control signal;

the first driver circuit is configured to receive the enable control signal, the first test flag signal, the first fixed level signal, the first OP and the second OP; and in response to that the semiconductor memory is in the preset test mode, control, in a case where the enable control signal is in the first level state, the impedance of the DM pin based on the first OP or the second OP according to a level state of the first test flag signal; or control, in a case where the enable control signal is in the second level state, the DM pin to be in the high impedance state through the first fixed level signal;

wherein when the fourth OP is in the first state, the enable control signal is in the first level state; when the fourth OP is in the second state, the enable control signal is in the second level state; when the third OP is in the third state, the first test flag signal is in the first level state; and when the third OP is in the fourth state, the first test flag signal is in the second level state.

10. The semiconductor memory according to claim 9, wherein the semiconductor memory is further configured to determine a first non-test mode control signal, a second impedance control signal and a first calibration signal; wherein the first calibration signal is configured to calibrate a pull-up resistance value, and the first driver circuit comprises:

a first signal processing module, configured to receive the first test flag signal, the enable control signal, the first fixed level signal, the first OP, the second OP and the first non-test mode control signal; and output, based on one of the first fixed level signal, the first OP and the second OP, a first impedance control signal according to the level state of the first test flag signal and the level state of the enable control signal in response to that the semiconductor memory is in the preset test mode; or output, based on the first non-test mode control signal, the first impedance control signal in response to that the semiconductor memory is not in the preset test mode;

a first logic module, configured to receive the first impedance control signal, the second impedance control signal and the first calibration signal; and select and logically combine the first impedance control signal, the second impedance control signal and the first calibration signal to output a first target signal; and

a first driver module, comprising a plurality of first impedance units and configured to receive the first target signal, and control the plurality of first impedance units by using the first target signal, so as to control the impedance of the DM pin;

wherein the first non-test mode control signal is configured to indicate an impedance of the DM pin in a mode except the preset test mode, and the second impedance control signal is configured to indicate an impedance of the data pin in the output driver state; or the first non-test mode control signal is configured to indicate the impedance of the data pin in the output driver state, and the second impedance control signal is configured to indicate the impedance of the DM pin in the mode except the preset test mode.

11. The semiconductor memory according to claim 10, wherein the first signal processing module comprises:

a third decoding module, configured to receive the first OP, decode the first OP and output a first decoded signal;

a fourth decoding module, configured to receive the second OP, decode the second OP and output a second decoded signal;

a first selection module, configured to receive the first test flag signal, the first

decoded signal and the second decoded signal; and select, according to the first test flag signal, one of the first decoded signal and the second decoded signal to output a first preselection signal;

a second selection module, configured to receive the enable control signal, the first preselection signal and the first fixed level signal; and select, according to the level state of the enable control signal, one of the first preselection signal and the first fixed level signal to output a first test mode control signal; and

a third selection module, configured to receive the test enable signal, the first test mode control signal and the first non-test mode control signal; and select, according to the level state of the test enable signal, one of the first test mode control signal and the first non-test mode control signal to output the first impedance control signal; wherein the test enable signal is configured to indicate whether the semiconductor memory is in the preset test mode.

12. The semiconductor memory according to claim 11, wherein each of the first decoded signal, the second decoded signal, the first preselection signal, the first fixed level signal, the first test mode control signal, the first non-test mode control signal and the first impedance control signal comprises an (M+1)-bit sub-signal, the first selection module comprises (M+1) first data selectors, the second selection module comprises (M+1) second data selectors, and the third selection module comprises (M+1) third data selectors; wherein

an input end of one first data selector receives a 1-bit sub-signal of the first decoded signal and a 1-bit sub-signal of the second decoded signal, an output end of one first data selector is configured to output a 1-bit sub-signal of the first preselection signal, and control ends of all the first data selectors receive the first test flag signal;

an input end of one second data selector receives the 1-bit sub-signal of the first preselection signal and a 1-bit sub-signal of the first fixed level signal, an output end of one second data selector is configured to output a 1-bit sub-signal of the first test mode control signal, and control ends of all the second data selectors receive the enable control signal;

an input end of one third data selector receives a 1-bit sub-signal of the first test mode signal and a 1-bit sub-signal of the first non-test mode control signal, an output end of one third data selector is configured to output a 1-bit sub-signal of the first impedance control

signal, and control ends of all the third data selectors receive the test enable signal;

wherein M is a positive integer.

13. The semiconductor memory according to claim 12, wherein the second impedance control signal comprises an (M+1)-bit sub-signal, the first calibration signal comprises N-bit sub-signals, the first target signal comprises I groups of sub-signals, and each group of sub-signals comprises N-bit sub-signals; the first driver module comprises I first impedance units, and each first impedance unit is configured to receive a group of sub-signals in the first target signal;

the first logic module is specifically configured to determine whether the level pull-up function of the at least one first impedance unit is enabled according to the first impedance control signal and the second impedance control signal; and

determine, in a case where an level pull-up function of an ith first impedance unit is enabled, a level state of an ith group of sub-signals in the first target signal according to the first calibration signal, so as to control a resistance value of the ith first impedance unit to be a standard resistance value; or determine, in a case where the level pull-up function of the ith first impedance unit is disabled, that the ith group of sub-signals in the first target signal are in the first level state;

wherein i, N and I are all integers, i is less than or equal to I, and (M+1) is less than or equal to I.

14. The semiconductor memory according to claim 13, wherein each first impedance unit comprises N first switch transistors, N second switch transistors and 2N first resistors;

a control end of an nth first switch transistor in an ith first impedance unit is connected with an nth sub-signal in the ith group of sub-signals in the first target signal, a first end of one first switch transistor is connected with a first end of one first resistor, and a second end of one first switch transistor is connected with a power signal;

a control end of one second switch transistor is connected with a second fixed level

signal, a first end of one second switch transistor is connected with a ground signal, a second end of one second switch transistor is connected with the first end of one first resistor, and second ends of 2N first resistors are all connected with the DM pin;

wherein n is an integer, and n is less than or equal to N.

15. The semiconductor memory according to claim 14, wherein

the first switch transistor is a P-channel field effect transistor, and the second switch transistor is an N-channel field effect transistor; a control end of the P-channel field effect transistor is a gate, a second end of the P-channel field effect transistor is a source, a first end of the P-channel field effect transistor is a drain, a control end of the N-channel field effect transistor is a gate, a second end of the N-channel field effect transistor is a drain, and a first end of the N-channel field effect transistor is a source;

the first level state is a high level state, the second level state is a low level state, sub-signals in the first fixed level signal are high-level signals, and the second fixed level signal is a low-level signal; and

the standard resistance value is 240 ohms.

16. An electronic device, comprising the semiconductor memory according to any one of claims 7-15.