

ABSTRACT

A memory apparatus includes an instruction memory and a plurality of micro control units. The instruction memory outputs a plurality of instruction codes at a predetermined time interval in accordance with a plurality of address signals and a plurality of divided clock signals. The plurality of micro control units are coupled to each of a plurality of memory regions, provide each of the plurality of address signals to the instruction memory in accordance with each of the plurality of divided clock signals, and perform operations in accordance with corresponding instruction codes among the plurality of instruction codes.

FIG. 6