

STRUCTURE AND METHOD FOR A SRAM CIRCUIT

ABSTRACT

The present disclosure provides an integrated circuit formed in a semiconductor substrate. The integrated circuit includes a first static random access memory (SRAM) cell having a first cell size; and a second SRAM cell having a second cell size greater than the first cell size. The first SRAM cell includes first n-type field effect transistors (nFETs) each having a first gate stack. The second SRAM cell includes second nFETs each having a second gate stack different from the first gate stack.

Figure 1