

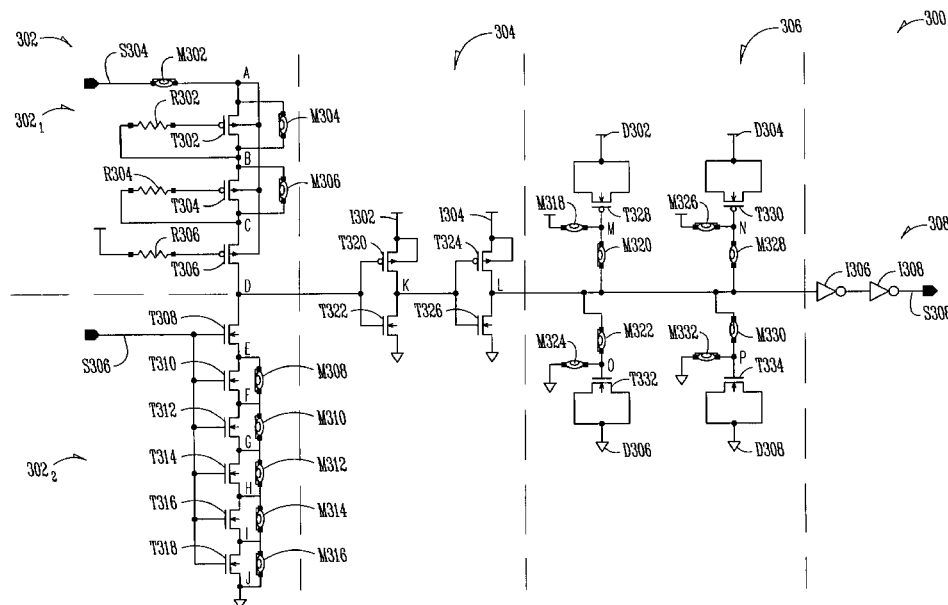


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- with international search report
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(54) Title: PROTECTION FOR INPUT BUFFERS OF FLASH MEMORIES



(S7) Abstract: An input buffer is discussed that inhibits semiconductor breakdown of thin gate-oxide transistors in low-voltage integrated circuits. One aspect of the input buffer includes an input stage having a gate, a drain, and a source. The gate of the input stage is receptive to an inhibiting signal, and the drain is receptive to an input signal. The input stage inhibits the input signal from being presented at the source of the input stage when the inhibiting signal is at a predetermined level. The input buffer further includes an output stage having an inverter that includes a first connection and a second connection. The first connection couples to the source of the input stage, and the second connection presents the input signal to a low-voltage flash memory device.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.